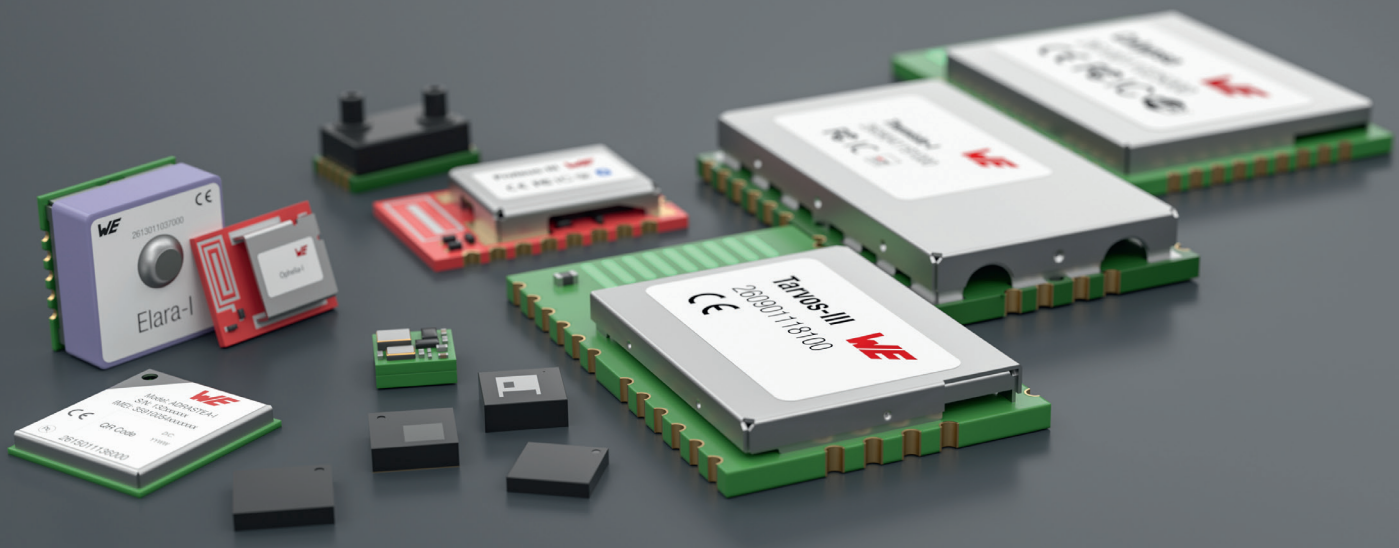

User manual

Adrastea-I

2615011136000

Version 1.8

January 20, 2026

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

****

MUST READ

Check for firmware updates

Before using the product, make sure you use the most recent firmware version, data sheet, and user manual. This is especially important for Wireless Connectivity products that were not purchased directly from Würth Elektronik eiSos. A firmware update on these respective products may be required.

We strongly recommend including the possibility of a firmware update in the customer system design.

Certification Information:

The certification information is mandatory to check, see chapter 3.3

Power Saving Features:

The power saving features information is important to check before enabling 3GPP defined eDRX and PSM features, see chapter 7.2, chapter 7.3, chapter 7.4

Application MCU:

Effective January 1, 2026, Sony will discontinue support for Open MCU for all new designs based on the ALT1250 chipset. As a result, using the integrated Arm Cortex M4 MCU of Adrastea-I for new application development is not recommended.

However, using Adrastea-I as a modem is not affected by this announcement.

Contents

1 Revision history

Manual version	FW version	HW version	Notes	Date
1.0	ADRASTEA-I_06.006	1.0	• Initial release of the manual	April 2022
1.1	ADRASTEA-I_06.006	1.0	• Added section `Adrastea-I GCF Certification`. • Added section `Minimal pin connections`. • Updated section `Application MCU`.	May 2023
1.2	ADRASTEA-I_06.006	1.0	• Actualized section `Regulatory compliance information`.	August 2023
1.3	ADRASTEA-I_06.006	1.0	• Updated information about GNSS update rate in section `GNSS: Time To First Fix`. • Updated GPIO Pin Information in section `GPIO Pin Information`. • Redundant sections 3.11 and 3.12 removed. Content can be found in section `GPIO Pin Information` and `E-JTAG Debug port`. • Updated information about bootdelay configurations in section `UART Default Configuration`.	August 2024

Continued on next page

1.3	ADRASTEA-I_06.006	1.0	• Added new section `DH0 Mode Setting`. • Added new section `DH1 Mode Setting`. • Added new section `DH2 Mode Setting`. • Updated link for Sony MCU access request in section `Application MCU`. • Updated section `Select LTE-M or NB-IoT Mode`. • Updated figure with more dimentions in section `Footprint`. • Added information about LTE antenna in section `Antenna solutions`. • Updated General labelling information for Adrastea-I in section `General labeling information`. • Added Information for explosion protection for Adrastea-I in section `Information for explosion protection`. • `Abbreviations` section updated.	August 2024
1.4	ADRASTEA-I_06.006	1.0	• Added chapter `Product testing` • Added chapter `Important notice UKCA` • Removed chapter "LOT number"	October 2024

1.5	ADRASTEA-I_06.006	1.0	• Removed iotcreator connectivity information • Updated information in section Benefits of Deutsche Telekom Certified Module • Updated information in Chapter Pinout • Updated information in Chapter GPIO Pin Information • Updated information in Chapter Functional description • Added Lot number information Chapter Lot number	April 2025
1.6	ADRASTEA-I_06.006	1.0	• Added EN 301 489-52 to Regulatory compliance information. • Added TLS Version information to Module Key Features. • Updated Minimal pin connections picture with SIM card holder to Minimal pin connections. • Updated SIM information in to Minimal pin connections. • Added extra step to check internet connection in to Register to Network. • Added information about ISO 7816 information in to SIM Pin Interface.	July 2025

1.7	ADRASTEA-I_06.006	1.0	• Added RED-DA (EN 13081) statement and supporting sections to `Regulatory compliance information` chapter.	August 2025
1.8	ADRASTEA-I_06.006	1.0	• Updated Application MCU information `Application MCU`, `Introduction`, `Module Key Features` chapters.	January 2026

2 Abbreviations

Abbreviation	Name
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
ASCI	Advanced Speech Call Items
APN	Access Point Name
BCD	Binary Coded Decimal
CLK	Clock signal
DH	Deep Hibernation
eDRX	Extended Discontinuous Reception
EJTAG	Embedded Joint Test Action Group
GLONASS	Global Navigation Satellite System
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GPIO	General Purpose Input Output
I^2C	Inter-Integrated Circuit
IoT	Internet of Things
IMEI	International Mobile station Equipment Identity
IMEISV	International Mobile station Equipment Identity and Software Version number
JTAG	Joint Test Action Group
LTE	Long Term Evolution
MCU	Micro controller Unit
MISO	Master In Slave Out
ME	Mobile Equipment
MOSI	Master Out Slave in
MT	Mobile Termination
MTU	Maximum Transfer Unit
PA	Power Amplifier
PD	Power Down
PMU	Power Management Unit
PSM	Power Save Mode
RAM	Random Access Memory
RAT	Radio Access Technology
RLP	Radio Link Protocol
RTC	Real Time Clock

SINAD	Signal to Noise and Distortion ratio
SIM	Subscriber Identity Module
SPI	Serial Peripheral Interface
SVN	Software Version Number
TA	Terminal Adaptor
TCXO	Temperature Compensated Crystal Oscillator
TE	Terminal Equipment
TTFF	Time To First Fix
UART	Universal Asynchronous Receiver/Transmitter
UE	User Equipment
UICC	Universal Integrated Circuit Card
USIM	Universal Subscriber Identity Module
XO	Crystal Oscillator

3 Introduction

Adrastea-I module is a compact LTE-M/NB-IoT Cellular module with integrated GNSS.

Based on the Sony Altair ALT1250 chipset, the Adrastea-I module provides AT-Command based multi-band configurability enabling international multi-regional coverage in LTE Cat M1 / NB1 radio access technologies.

Adrastea-I includes a fully integrated global navigation satellite system solution that supports GPS and GLONASS positioning systems.

Compact 13.4mm x14.6mm x 1.85mm design allows the module to fit in small-size applications.

The module can be operated through one of two available cellular communication technologies:

- LTE-Cat.M or
- LTE-Cat.NB-IoT.

The Adrastea-I EV-Kit and "Adrastea Commander" tool ([1]) allow getting started with the module and testing its functionalities. The EV-Board can be connected to an USB port of a PC. The EV-Board also represents our reference design. For further information, Refer to the EV-Board manual [2].

The module comes with the declaration of conformity (CE), is compliant to RoHS, REACH. The Adrastea-I module is GCF and Deutsche Telekom certified.

Figure 1: Adrastea-I

3.1 Adrastea-I GCF Certification

Adrastea-I is GCF certified module. Major advantage with GCF certified module integrated in end IoT application is that it reduces efforts for industry and operator specific certifications. However, customer shall check certification requirements with network operator before commercial deployment of IoT devices.

GCF™
Global Certification Forum

CERTIFICATE

The Global Certification Forum Ltd advises that
Würth Elektronik eiSos GmbH & Co. KG

has successfully demonstrated compliance
with the GCF certification requirements of GCF-CC

For
Adrastea-I
IoT Module

On
20-Mar-2023

GCF CC Version:	Status:	GCF Ref. Number:
3.87.0	**Published**	**11367**

This certificate has been issued by the Global Certification Forum in accordance with the requirements of the GCF PRDs. For the actual status of a device certification, please refer to the GCF web site.

The device manufacturer confirms that they are solely responsible for certifying the product and holds the GCF entirely harmless from any responsibility or liability associated with the product and/or the certification process. All GCF marks and/or certificates are provided "as is" with no representation and GCF expressly disclaims all warranties whatsoever whether express, implied statutory or otherwise. In no event shall GCF be liable for any direct, indirect, consequential or any damages whatsoever in any way connected with the use or performance of any GCF certified product whether based on contract, tort, negligence, strict liability or otherwise.

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Figure 2: Adrastea-I GCF Certification

3.2 Adrastea-I Deutsche Telekom Certification

Adrastea-I is certified by Deutsche Telekom.

To Würth Elektronik
Forward to Ravindra Singh
From Miguel Rodriguez (Deutsche Telekom AG)
Contact E-Mail: miguel.rodriguez@telekom.de
Date 07th February, 2022
Subject Limited Certification for Würth Elektronik ADASTREA-I Communication Module

Dear Würth Elektronik Team,

Deutsche Telekom issues a limited certification for your ADASTREA-I communication module:

Concept Class	LPWA-enabled, multi-mode module (NB1, LTE-M)
Deutsche Telekom (DT) Certification Date	07.02.2022
DT Responsible Entity / Contact	VTI-IOT / Miguel Rodriguez
Certified Deutsche Telekom Affiliates*	**(Limited) NB-IoT:** AT, CZ, DE, HR, NL, PL, SK **(Limited) LTE-M:** AT, DE, NL
OEM Firmware Version	ADRASTEA-I_06.006
OEM Hardware Version	V1.0

* Please refer to the OEM Certification Report for Deutsche Telekom Affiliate Country Codes.

Detailed conditions for this limited certification are listed below. Until these topics are addressed, a full technical certification is not granted by Deutsche Telekom. For more details, please refer to the OEM Certification Report of this product.

- OEM is required to present GCF certification for this product.

Deutsche Telekom considers this product to be suitable for IoT projects having large volumes, as there is support for the no-harm to network / communication efficiency feature GSMA TS.34 Radio Policy Manager (RPM).

Kind regards,
Deutsche Telekom AG

Miguel Rodriguez
Digital unterschrieben von Miguel Rodriguez
Datum: 2022.02.07 15:10:05 +01'00'

Miguel Rodriguez
Sr. Mgr., IoT Device Verification & Engineering

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Board of Directors Adel Al-Saleh, Birgit Bohle, Srinivasan Gopalan, Dr. Christian P. Illek, Thorsten Langheim, Dominique Leroy, Claudia Nemat

Commercial register Amtsgericht Bonn HRB 6794
Registered office Bonn

VAT ID No. DE 123475223
WEEE Reg.-No. DE50478376

Figure 3: Adrastea-I Deutsche Telekom Certification

3.3 Benefits of Deutsche Telekom Certified Module

Normal Cellular Cerfication procedure includes 3 different types of certifications:

- Regulatory Certification: CE, FCC and similar based on region.
- Industry Specific Certification: GCF, PTCRB
- Network Operator Certification: Vodafone, Deutsche Telekom, AT&T etc.

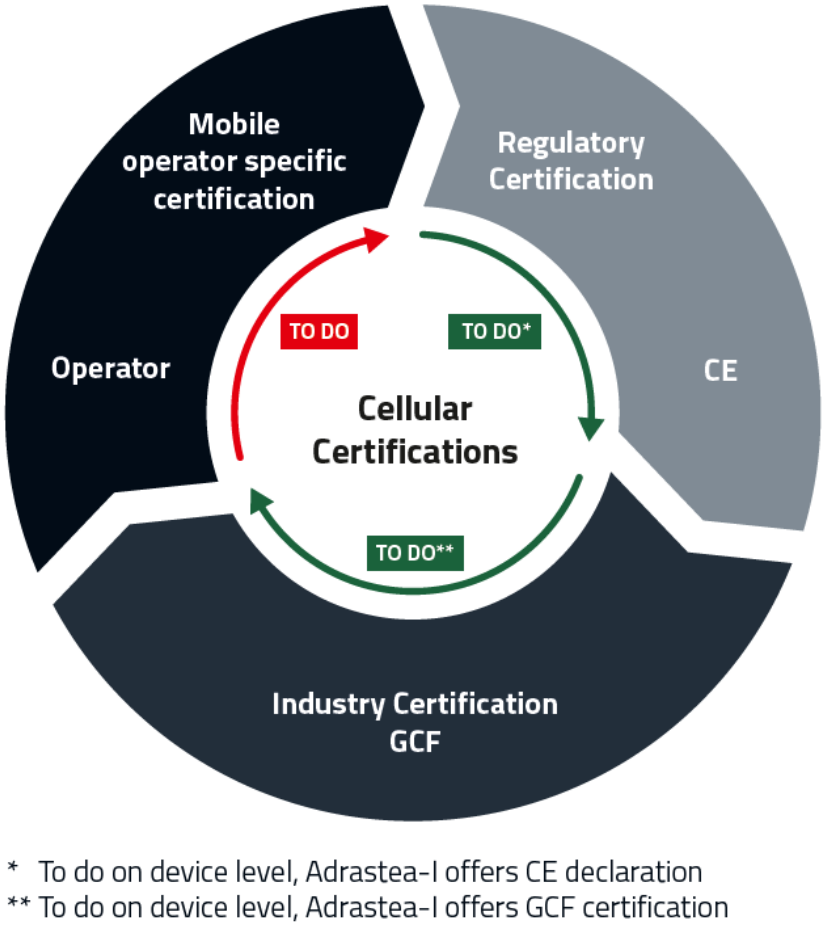


Figure 4: Normal Cellular Certification Process

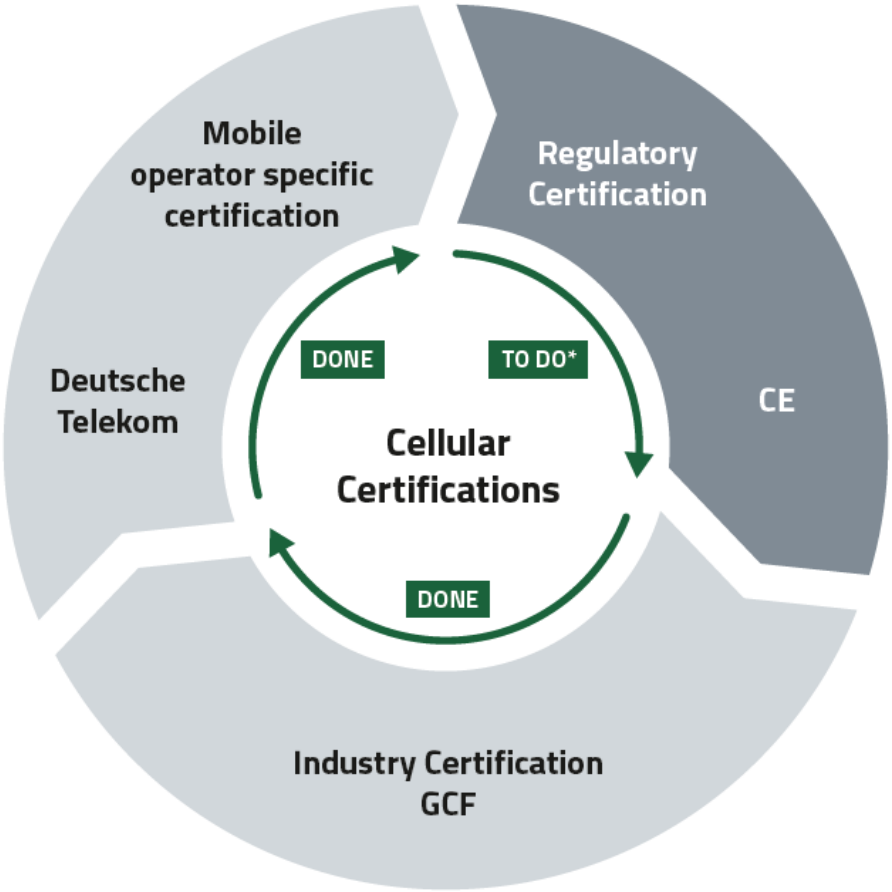
Pre-Certified Adrastea-I module from Deutsche Telekom brings the following key advantages:

- It enables integration to end device without further end device label Industry specific Certification (i.e. GCF) and Network Operator Certification (Deutsche Telekom).

Regulatory Certifications (i.e. CE, FCC and similar based on region) are still required for the end product.

- Obtain assurance: Pre-certified module reduces the final test effort.
- Save time and money: The end product does not require to go through complex cellular certification process again.

The benefits of certification are applicable exclusively when the customer utilizes connectivity (IoT SIM cards) provided by Deutsche Telekom. To obtain the certification benefits, the customer must use connectivity (IoT SIM cards) from Deutsche Telekom. It is required that the customer contacts Deutsche Telekom to acquire the necessary IoT SIM cards.



*To do on device level, Adrastea-I offers CE declaration

Figure 5: Benefits of Deutsche Telekom Certified Module

3.4 Module Key Features

Feature	Description
Physical Dimensions	13.4mm x 14.6mm x 1.85mm
Supported Networks	- LTE-Cat.M - LTE-Cat.NB-IoT
LTE Supported Bands	**LTE-Cat.M:** B2/B3/B4/B5/B8/B12/B20/B25/B26/B28 **LTE-Cat.NB-IoT:** B3/B5/B8/B20/B28
Module Interfaces	- USIM - UART - I^2C Master - SPI Master - GPIO - ADC - JTAG
Integrated GNSS	Adrastea-I includes a fully integrated global navigation satellite system solution that supports GPS and GLONASS positioning system.
Output Power class	Power Class 3 (23 dBm)
Maximum Data Rate	**LTE-Cat.M:** Downlink: 300 Kbps, Uplink: 375 Kbps
	LTE-Cat.NB-IoT: Downlink: 27.2 Kbps, Uplink: 62.5 Kbps
3GPP Standard Compliance	3GPP Release 13 compliant, Upgradable to Rel 14
Firmware Upgrade	- Secure Firmware upgrade over UART - Secure Firmware upgrade over air
Supported Protocols	- IPv4, IPv6 - TCP/UDP SOCKET - HTTP/HTTPS - TLS/DTLS (TLS Version 1.2) - LWM2M Client - MQTT
AT Commands	3GPP TS 27.007 and 3GPP TS 27.005 AT commands, as well as Würth Elektronik eiSos enhanced AT commands
Operating Voltage	- VDD: From 2.3 V to 4.3 V - VDD_FEM: From 3.1 V to 4.3 V
Temperature Range	Operation temperature: -40 °C to +85 °C

Table 3: Module Key Features

3.5 Block diagram

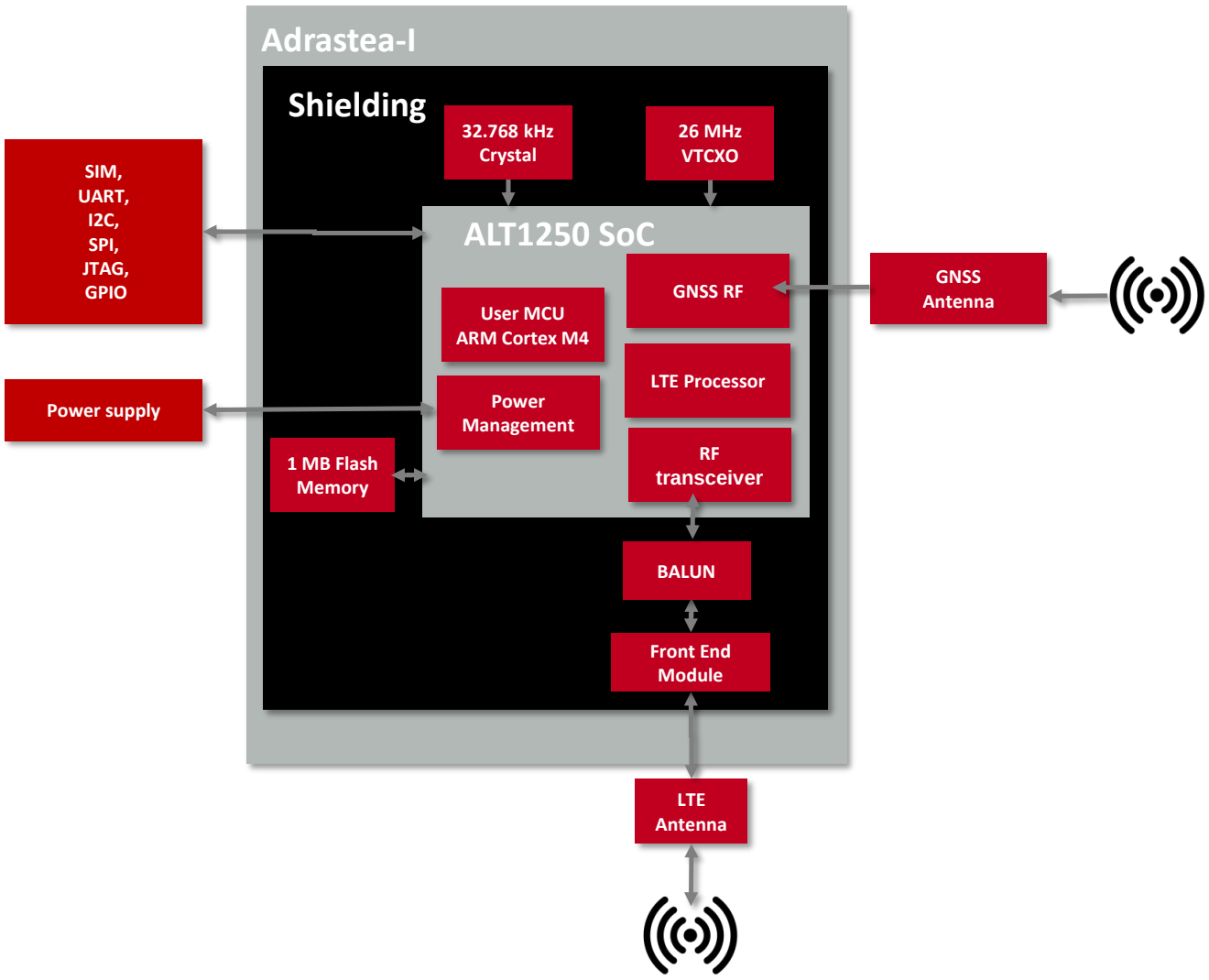


Figure 6: Block diagram

3.6 Ordering information

WE order code	Description
2615011136000	Cellular LTE-M/NB-IoT module in T&R packaging
2615029236001	Cellular LTE-M/NB-IoT EV-Kit

Table 4: Ordering information

4 Electrical and Radio Specifications

Unless otherwise stated, all the values given in the manual were measured on the Adrastea-I EV-Board under the following conditions: T = 25 ℃ and powered via 5 V/1A Power Jack. The voltage regulator of the EV-Board regulates the connected voltage 5 V down to 3.6 V and supplies the remaining parts of the circuit. If the EV-Board is power sourced, the power LED1 lights up.

4.1 Operating Conditions

Parameter	Direction	Min.	Typ.	Max.	Unit
Supply voltage (VDD)	Supply	2.3	3.6	4.3	V
Supply voltage (VDD_FEM)	Supply	3.1	3.6	4.3	V
VSIM	Output	1.7	1.8	1.9	V
VDDIO	Output	1.7	1.8	1.9	V
Operating temperature		-40	25	85	℃

Table 5: Operating conditions

4.2 Current Consumption

4.2.1 LTE-Cat.M Mode

Description	Test Condition	Value	Unit
LTE-IDLE	MCU RUN	16.8	mA
	MCU SHUTDOWN	2.9	mA
Peak Current (TX)	TX @23dBm, MCU RUN	454.2	mA
PSM Current (DH0)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	1.57	µA
PSM Current (DH1)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	39.6	µA
PSM Current (DH2)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	82.2	µA
GNSS-Active	MCU RUN, LTE RF Disabled (AT+CFUN=0)	53.98	mA

Table 6: LTE-Cat.M Current consumption

4.2.2 LTE-Cat.NB-IoT Mode

Description	Test Condition	Value	Unit
LTE-IDLE	MCU RUN	15.7	mA
	MCU SHUTDOWN	2.8	mA
Peak Current (TX)	TX @23dBm, MCU RUN	434	mA
PSM Current (DH0)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	1.57	µA
PSM Current (DH1)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	38.5	µA
PSM Current (DH2)	MCU SHUTDOWN, LTE RF Disabled (AT+CFUN=0)	81.5	µA

Table 7: NB-IoT Current consumption

4.3 LTE Radio Characteristics

Module performance is based on the quality of the RF link from LTE network to the Adrastea-I module.

The following factors and tasks are critical for the performance of the Adrastea-I module:

- External LTE antenna for signal reception from LTE network.
- RF trace delivering the signal from the external antenna to the LTE RF pad of the Adrastea-I module
- Minimization of external and environmental effects.

4.3.1 LTE Supported Bands

4.3.2 LTE-Cat.M Mode

Band	Transmit Band (Tx)	Receive Band (Rx)	Unit
B2	1850 - 1910	1930 - 1990	MHz
B3	1710 - 1785	1805 - 1880	MHz
B4	1710 - 1755	2110 - 2155	MHz
B5	824 - 849	869 - 894	MHz
B8	880 - 915	925 - 960	MHz
B12	699 - 716	729 - 746	MHz
B20	832 - 862	791 - 821	MHz
B25	1850 - 1915	1930 - 1995	MHz
B26	814 - 849	859 - 894	MHz
B28	703 - 748	758 - 803	MHz

Table 8: LTE-Cat.M Supported Bands

4.3.3 LTE-Cat.NB-IoT Mode

Band	Transmit Band (Tx)	Receive Band (Rx)	Unit
B3	1710 - 1785	1805 - 1880	MHz
B5	824 - 849	869 - 894	MHz
B8	880 - 915	925 - 960	MHz
B20	832 - 862	791 - 821	MHz
B28	703 - 748	758 - 803	MHz

Table 9: LTE-Cat.NB-IoT Supported Bands

4.3.4 RF Receiving Sensitivity

Unless noted otherwise, the Adrastea-I evaluation boad is in static mode, values were measured with Rohde and Schwarz CMW500 equipment.

4.3.5 LTE-Cat.M Reference sensitivity

Band	Band Width	Value	Unit
B2	1.4 MHz	-105	dBm
B3	1.4 MHz	-106.4	dBm
B4	1.4 MHz	-106.2	dBm
B5	1.4 MHz	-106.2	dBm
B8	1.4 MHz	-107.2	dBm
B12	1.4 MHz	-105.6	dBm
B20	1.4 MHz	-106.4	dBm
B25	1.4 MHz	-106.8	dBm
B26	1.4 MHz	-106.4	dBm
B28	1.4 MHz	-106	dBm

Table 10: LTE-Cat.M RX Sensitivity

4.3.6 LTE-Cat.NB-IoT Reference sensitivity

Band	Value	Unit
B3	-110	dBm
B5	-110	dBm
B8	-110	dBm
B20	-110	dBm
B28	-110	dBm

Table 11: LTE-Cat.NB-IoT RX Sensitivity

4.3.7 Maximum Output Power

Unless noted otherwise, the Adrastea-I evaluation boad is in static mode, values were measured with Rohde and Schwarz CMW500 equipment.

4.3.8 LTE-Cat.M Maximum Output Power

Band	Band Width	Value	Unit
B2	5 MHz	22.9	dBm
B3	5 MHz	21.5	dBm
B4	5 MHz	21.4	dBm
B5	5 MHz	21.7	dBm
B8	5 MHz	22.9	dBm
B12	5 MHz	21.4	dBm
B20	5 MHz	21.7	dBm
B25	5 MHz	23.0	dBm
B26	5 MHz	21.8	dBm
B28	5 MHz	21.9	dBm

Table 12: LTE-Cat.M Maximum Output Power

4.3.9 LTE-Cat.NB-IoT Maximum Output Power

Band	Value	Unit
B3	21.8	dBm
B5	22.0	dBm
B8	23.7	dBm
B20	22.1	dBm
B28	22.4	dBm

Table 13: LTE-Cat.NB-IoT Maximum Output Power

4.4 GNSS Radio Characteristics

Module performance is based on the quality of the RF link from GNSS satellites to the module.

The following factors and tasks are critical for the performance of the integrated GNSS:

- Free/unimpacted line of sight
- External GNSS antenna for signal reception from GNSS satellites
- RF trace delivering the signal from the external antenna to the RF pad of the GNSS module
- Minimization of external and environmental effects

Adrastea-I supports GPS and GLONASS satellite systems using dedicated hardware accelerators in a power and cost efficient manner. The GNSS receiver shares certain hardware resources with the modem. This enables GNSS measurement slots to be efficiently scheduled based on the modem link state. The device key target is to allow GNSS positioning for asset management applications where infrequent position updates are required.
The Adrastea-I GNSS shares the RF Rx path with the LTE modem and, therefore, cannot operate in parallel with LTE data transfer. Hence this GNSS is not suitable for products that inherently require this co-existence, LTE connection and GNSS tracking.

GNSS cannot co-exist with LTE data transfer. LTE communication has higher priority over GNSS and, therefore, GNSS is automatically shut down once LTE is active (if it was active). While LTE is active, GNSS cannot be activated and all GNSS AT commands are responded with error.

4.4.1 GNSS Supported Constellation

Adrastea-I supports the following constellation (Satellite systems):

- GPS
- GLONASS

4.4.2 GNSS: Operating frequencies

Description	Min	Typ.	Max	Unit
Input Frequency	1560		1610	MHz

Table 14: Radio characteristics

4.4.3 GNSS: Rx Sensitivity

Module sensitivity is the weakest signal level the receiver can work with and it depends on the state of the module.

- Cold start sensitivity is the minimum power required by the module to acquire satellites and perform first fix in cold start.
- Hot start sensitivity is the minimum power required by the module to acquire satellites and perform first fix in hot start.
- Tracking sensitivity is the minimum power required by the module to keep in track of the position fix.

Parameter	Test Condition	Value	Unit
Cold Start	GPS-GLONASS	-145	dBm
Hot Start	GPS-GLONASS	-152	dBm
Tracking	GPS-GLONASS	-160	dBm

Table 15: GNSS RX Sensitivity

4.4.4 GNSS: Time To First Fix

The Time To First Fix (TTFF) is the time needed by the module to achieve the first valid position fix, once the module is powered up or returns from a period of signal blockage.

GNSS update rate for Adrastea-I is 1 Hz (once per second).

Depending on the type of start (cold or hot), a different TTFF performance is given below.

Parameter	Test Condition	Value	Unit
Cold Start	GPS-GLONASS, Power Level = -120dBm	36	s
Hot Start	GPS-GLONASS, Power Level = -120dBm	1	s

Table 16: GNSS Time to First Fix

4.4.5 GNSS: Position Accuracy

Parameter	Test Condition	Value	Unit
Position Accuracy	GPS-GLONASS, Power Level = -120dBm	1.5	m

Table 17: GNSS Position Accuracy

5 Pinout

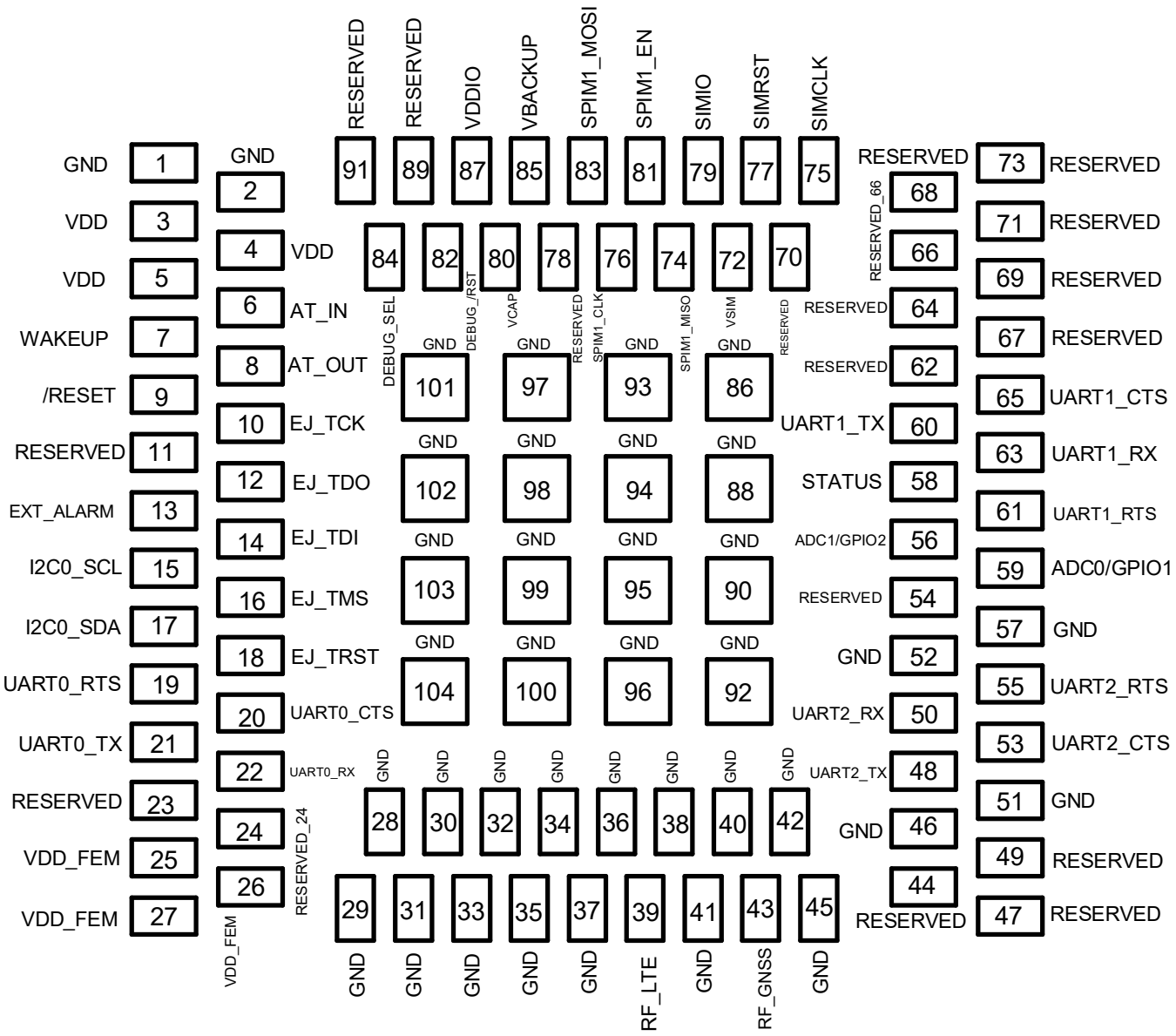


Figure 7: Pinout (top view)

Pin Number	Designation	I/O	Description
1	*GND*	Supply	Negative Supply Voltage
2	*GND*	Supply	Negative Supply Voltage
3	*VDD*	Supply	Power supply for module
4	*VDD*	Supply	Power supply for module
5	*VDD*	Supply	Power supply for module
6	*AT_IN*	Input	Anti-tamper input
7	*WAKEUP*	Input	Wakeup active high Default pull resistor at power up and after DH0: No pull DH2 state: No pull DH1 state: No pull DH0 state: No pull
8	*AT_OUT*	Output	Anti-tamper output
9	*/RESET*	Input	Reset active low
10	*EJ_TCK*	Input	JTAG Test Clock
11	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
12	*EJ_TDO*	Output	JTAG Test Data Output
13	*EXT_ALARM*	Output	Alarm Output
14	*EJ_TDI*	Input	JTAG Test Data Input
15	*I2C0_SCL*	Input/Output	I2C serial clock Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
16	*EJ_TMS*	Input	JTAG Test Mode Select
17	*I2C0_SDA*	Input/Output	I2C serial data Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
18	*EJ_TRST*	Input	JTAG Test Reset (required external pull down)

19	*UART0_RTS*	Output	MCU UART0 Request to Send Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
20	*UART0_CTS*	Input	MCU UART0 Clear to Send Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
21	*UART0_TX*	Output	MCU UART0 Transmit Data Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
22	*UART0_RX*	Input	MCU UART0 Receive Data Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
23	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
24	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
25	*VDD_FEM*	Supply	Power supply for FEM (Front End Module)
26	*VDD_FEM*	Supply	Power supply for FEM (Front End Module)
27	*VDD_FEM*	Supply	Power supply for FEM (Front End Module)
28	*GND*	Supply	Negative supply voltage
29	*GND*	Supply	Negative supply voltage

30	*GND*	Supply	Negative supply voltage
31	*GND*	Supply	Negative supply voltage
32	*GND*	Supply	Negative supply voltage
33	*GND*	Supply	Negative supply voltage
34	*GND*	Supply	Negative supply voltage
35	*GND*	Supply	Negative supply voltage
36	*GND*	Supply	Negative supply voltage
37	*GND*	Supply	Negative supply voltage
38	*GND*	Supply	Negative supply voltage
39	*RF_LTE*	RF	RF Signal LTE
40	*GND*	Supply	Negative supply voltage
41	*GND*	Supply	Negative supply voltage
42	*GND*	Supply	Negative supply voltage
43	*RF_GNSS*	RF	RF Signal GNSS
44	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
45	*GND*	Supply	Negative supply voltage
46	*GND*	Supply	Negative supply voltage
47	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
48	*UART2_TX*	Output	UART2 Transmit Data (CLI port)
49	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
50	*UART2_RX*	Input	UART2 Receive Data (CLI port)
51	*GND*	Supply	Negative supply voltage
52	*GND*	Supply	Negative supply voltage
53	*UART2_CTS*	Input	UART2 Clear to Send (CLI port)
54	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
55	*UART2_RTS*	Output	UART2 Request to Send (CLI port)
56	*ADC1/GPIO2*	Input/Output	Auxiliary Analog to Digital Converter Input/Programmable GPIO Default pull resistor at power up and after DH0: Pull Down DH2 state: SW configurable DH1 state: No pull DH0 state: No pull

57	*GND*	Supply	Negative supply voltage
58	*STATUS*	Output	Module Status
59	*ADC0/GPIO1*	Input/Output	Auxiliary Analog to Digital Converter Input /Programmable GPIO Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
60	*UART1_TX*	Output	UART1 Transmit Data (Modem Log port)
61	*UART1_RTS*	Output	UART1 Request to Send (Modem Log port)
62	*RESERVED*	–	Reserved
63	*UART1_RX*	Input	UART1 Receive Data (Modem Log port)
64	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
65	*UART1_CTS*	Input	UART1 Clear to Send (Modem Log port)
66	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
67	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
68	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
69	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
70	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
71	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
72	*VSIM*	Output	SIM Output voltage
73	*RESERVED*	–	Reserved (Shall be soldered but not connected.)

74	*SPIM1_MISO/ GPIO39*	Input/Output	MCU_SPIM1_MISO/Programmable GPIO Default pull resistor at power up and after DH0: Pull Down DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
75	*SIMCLK*	Output	SIM Clock
76	*SPIM1_CLK/ GPIO41*	Input/Output	MCU_SPIM1_CLK/Programmable GPIO Default pull resistor at power up and after DH0: Pull Down DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
77	*SIMRST*	Output	SIM Reset
78	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
79	*SIMIO*	Input/Output	SIM Data
80	*VCAP*	Input/Output	Connecting external capacitor as backup for VDD
81	*SPIM1_EN/ GPIO40*	Input/Output	MCU SPI Enable/ Programmable GPIO Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
82	*DEBUG_RST*	Input/Output	Reset pin for the JTAG probe
83	*SPIM1_MOSI/ GPIO38*	Input/Output	MCU_SPIM1_MOSI/ Programmable GPIO Default pull resistor at power up and after DH0: Pull Down DH2 state: SW configurable DH1 state: No pull DH0 state: No pull

84	*DEBUG_SEL*	Input	Reset pin for the JTAG probe
85	*VBACKUP*	Input	Input from backup battery
86	*GND*	Supply	Negative supply voltage
87	*VDDIO*	Output	Output Voltage (it will turn off at DH0 and DH1 sleep mode)
88	*GND*	Supply	Negative supply voltage
89	*RESERVED*	–	Reserved (Shall be soldered but not connected.)
90	*GND*	Supply	Negative supply voltage
91	*RESERVED*	–	Reserved(Shall be soldered but not connected.)
92	*GND*	Supply	Negative supply voltage
93	*GND*	Supply	Negative supply voltage
94	*GND*	Supply	Negative supply voltage
95	*GND*	Supply	Negative supply voltage
96	*GND*	Supply	Negative supply voltage
97	*GND*	Supply	Negative supply voltage
98	*GND*	Supply	Negative supply voltage
99	*GND*	Supply	Negative supply voltage
100	*GND*	Supply	Negative supply voltage
101	*GND*	Supply	Negative supply voltage
102	*GND*	Supply	Negative supply voltage
103	*GND*	Supply	Negative supply voltage
104	*GND*	Supply	Negative supply voltage

Table 18: Pinout

5.1 Module Power Up

An automatic power up sequence occurs when connecting the device to the power supply (VDD). The automatic power up sequence consists of the following phases:

- Phase 0: RET LDO to ramp up for supplying 1.0V retention core domain.
- Phase 1: I/O LDO to ramp up for supplying 1.8 V I/O domain.
- Phase 2: RF LDO to ramp up for supplying 1.9V RF domain.
- Phase 3: DCDC to ramp up for supplying 1.3V of Digital LDO and RF.
- Phase 4: DIG LDO to ramp up for supplying 1.0V of digital core domain.
- Phase 5: FLASH LDO to ramp up for supplying 1.8 V of Flash Domain.

Regulators will start ramping only with 1us delay from power good indication of previous phase. The automatic power up sequencing is shown below:

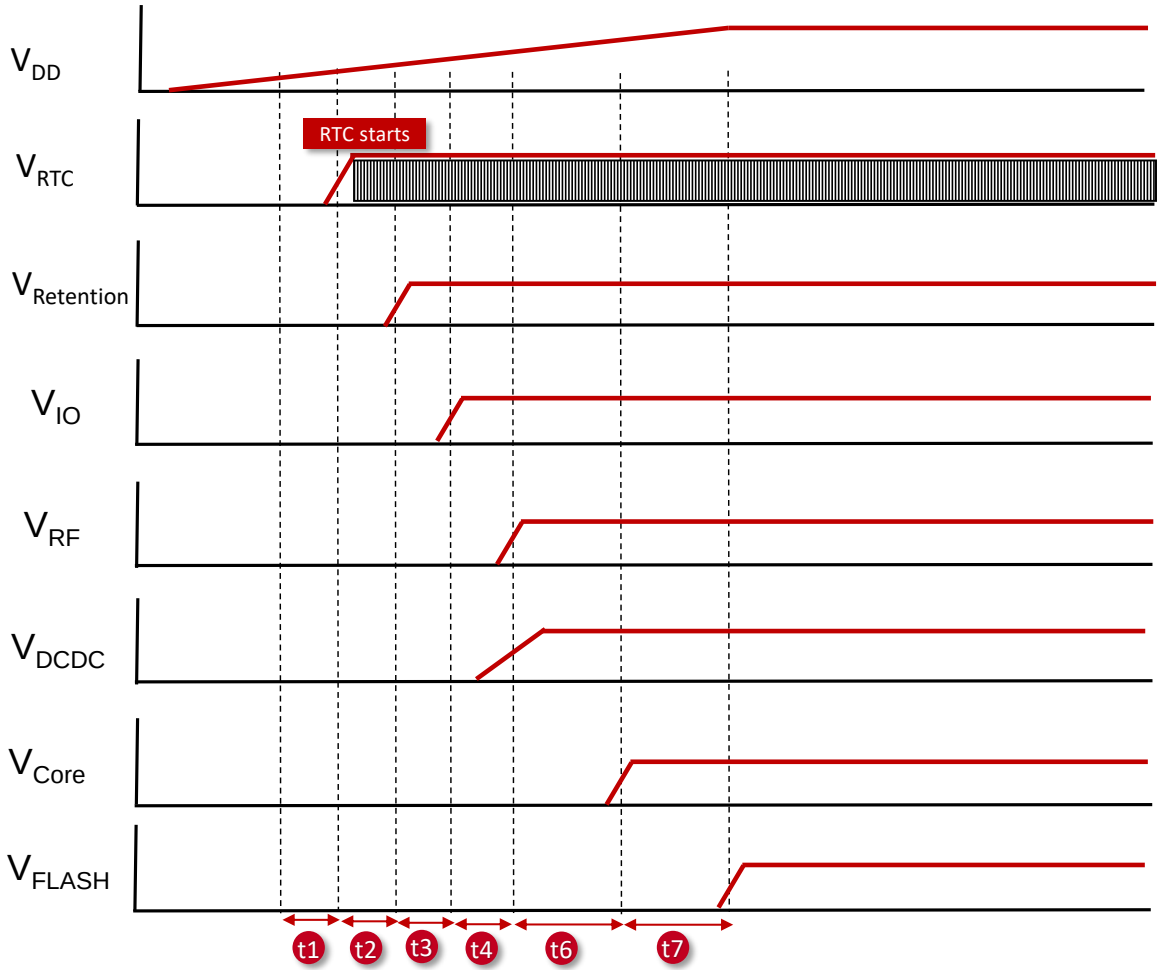


Figure 8: Adrastea-I Power up Sequence

Parameter	Description	Min.	Max.	Unit
t1	When VDD crosses the 0.8V threshold-VRTC should follow the VDD unless it has some capacitance on it.	0	5	µs
t2	Digital retention power up, the VDD slew rate has impact on this timing.	70	100	µs
t3	I/O LDO power up.	10	60	µs
t4	RF LDO power up.	10	60	µs
t5	DCDC boot time.	100	200	µs
t6	Core LDO power-up.	10	60	µs
t7	FLASH LDO power-up.	10	60	µs

Table 19: Power Up timing

5.2 Module Power Down

Power down sequence of the regulators will occur in following conditions:

- Turn off VDD.
- Shutdown is requested by */RESET* pin pulled to low.

5.3 Module Reset

Module reset will occur in following conditions:

- Perform power cycle - Turn off/on VDD and power up the device from reset state.
- Using */RESET* pin user can initiate power cycle that resets the device.

5.4 WAKEUP pin

This pin can be used to immediately wake up the module when being in low power state. This pin allows the module to get out of sleep mode when pulled HIGH.

The host connected to this pin should always keep the state of this pin (HIGH/LOW) at a known state (not floating) according to the required functionality.

- Pulled HIGH: Wake up internal MCU of module from sleep mode.
- Pulled LOW: Allowing internal MCU of module to go into sleep mode.

5.5 AT_IN and AT_OUT pins

User can connect the AT_OUT pin to the AT_IN pin in order to protect a device or module from tampering. The device will generate a software indication if the AT_OUT and AT_IN pins are disconnected.

The anti-tampering mechanism works in all active modes and all DHx power saving modes.
If the anti-tampering is not in use, the AT_IN should be shorted to GND.

5.6 /RESET pin

This pin has the highest priority compared to other chip functionalities, therefore asserting it will always force a hard reset. This pin is with internal PU resistor to 1.8V.

- Pulled HIGH: Turn on module regulators and power up the module.
- Pulled LOW: Turn off module regulators and shutdown the module.
- LOW to HIGH: Reset module (keep holding for at least 100 ms on LOW level before changing to HIGH).

5.7 EXT_ALARM pin

The EXT_ALARM pin can be used as an alarm indicator to an external host as per the Adrastea-I power mode. The behavior is as below:

Module State	Test Condition	EXT_ALARM Pin Expected behavior
DH0	MCU Shutdown, AT+CFUN=0	High Impedance
DH1	MCU Shutdown, AT+CFUN=0	High Impedance
DH2	MCU Shutdown, AT+CFUN=0	LOW signal
Active	MCU RUN	HIGH signal

Table 20: EXT_ALARM Pin

5.8 RF_LTE pin

This is the LTE antenna pin. The impedance should be close to 50 Ω, VSWR (Voltage Standing Wave Ratio) < 1.5.

Connect 50 Ω transmission lines from this pin to the 50 Ω Primary Antenna/Antenna-connector. Refer to our hardware layout recommendations (chapter 9).

5.9 RF_GNSS pin

This is the GNSS antenna pin. The impedance should be close to 50 Ω, VSWR (Voltage Standing Wave Ratio) < 1.5.

Connect 50 Ω transmission lines from this pin to the 50 Ω Primary Antenna/Antenna-connector. Refer to our hardware layout recommendations (chapter 9).

5.10 VBACKUP and VCAP pins

Adrastea-I supports a battery backup mechanism which allows seamless replacement of a weak battery. The battery should be replaced after the device is placed in DH0 state, and only when the RTC circuitry is operational, and is applied by VRTC.
The VBACKUP pin (battery) or the VCAP (capacitor) can be used as a backup during replacement. The VCAP pin should be left floating if a battery backup is used, while the VBACKUP pin should be left floating if a capacitor backup is used. If the application does not require a battery then both the VBACKUP and the VCAP pins should be left floating.

5.10.1 VCAP pin

The capacitor value should be large enough to keep the VCAP supply voltage above 1.8 V for as long as it takes for the battery to be replaced. Equation 1 should be used for calculating the capacitor value (C_{CAP}).

Equation1:
$C_{CAP} = (I_{CAP} \times T)/(V_{to} - V_{MIN})$

The following parameters should be taken into account when making these calculations:

- The maximum current drawn from VCAP (I_{CAP} = 10uA).
- The maximum period of time (T) it should take for battery replacement.
- The voltage that the capacitor was charged to (V_{to}).
- The minimum voltage that the capacitor can discharge while still providing sufficient operational voltage for the RTC (V_{MIN} = 1.8 V).

Example:
If the capacitor is charged to 3.3 V, and battery replacement requires 30 seconds, then the capacitor should be at least 200 µF (see equation below).
$C_{CAP} = (10uA \times 30s)/(3.3\ V - 1.8\ V) = 200uF$

5.10.2 VBACKUP pin

There is an option to include an external battery that can maintain the system's supply for a very short time while the main supply (VDD) is absent. The intention is to use a coin battery which is non-rechargeable. VDD thresholds at which the capacitor will start to provide VRTC:

- Similar to VCAP thresholds (see in the above section `5.10.1`).
- Pull Low: Turn off module regulators and shutdown the module.
- In case a battery is not used, this pin should be left open (not connected).

5.10.3 VDDIO

1.8 V power to the retention's I/O.

VDDIO is turned off in DH0 and DH1 state. Therefore it is not allowed to provide external voltage to IOs.

5.11 Digital I/O Pins Specifications

These characteristics are applicable for VDDIO in the 1.7V - 1.9V range.

Parameter	Min.	Max.	Unit
Input LOW Level, input and I/O pins	GND	0.3 x VDDIO	V
Input HIGH Level, input and I/O pins	0.7 x VDDIO	VDDIO	V
Output LOW Level		0.2 x VDDIO	V
Output HIGH Level	0.8 x VDDIO		V
Input pull-up resistor resistance	13	45	KΩ
Input pull-up resistor current	11	44	µA
Input pull-down resistor resistance	13.6	45	KΩ
Input pull-down resistor current	11	43	µA

Table 21: Digital I/O Pins Specifications

The total current from all IOs combined, and supplied by VDDIO, should not exceed 50mA.

6 Module Interfaces

Adrastea-I interfaces and specific pin connections for different interfaces are described in this chapter.

6.1 UART Interface

Adrastea-I supports 3 UART interfaces.

UART Number	Description
UART0	MCU UART, this interface is used for AT Commands.
UART1	This interface is used to capture modem logs.
UART2	This interface is used for MCU and Modem Firmware upgrade

Table 22: UART Interfaces

6.1.1 UART Default Configuration

UART	Function	Baud rate	Data	Parity	Stop	Flow Control
UART0	MCU UART	115200	8bit	None	1bit	Hardware RTS/CTS (default None)
UART1	Modem Log Port	921600	8bit	None	1bit	Hardware RTS/CTS (default None)
UART2	Firmware upgrade (CLI Port)	115200	8bit	None	1bit	Hardware RTS/CTS (default None)

Table 23: UART Default Configuration

UART1 is used to capture the modem logs.
UART2 is used for local firmware upgrades.

UART0 is required to send the AT command for boot delay setting (AT%SETBDELAY=10) before accessing the UART2 for firmware update.

Flow control is needed for firmware upgrade.

UART communication is not possible when Adrastea-I is in deep hibernate mode (DH0, DH1 and DH2).

6.1.2 UART0 Pin Interface

Pin Number	Designation	I/O	Description	Electrical Characteristic
19	*UART0_RTS*	Output	MCU UART0 Request to Send	1.8 V
20	*UART0_CTS*	Input	MCU UART0 Clear to Send	1.8 V
21	*UART0_TX*	Output	MCU UART0 Transmit Data	1.8 V
22	*UART0_RX*	Input	MCU UART0 Receive Data	1.8 V

Table 24: UART0 Pin Interface

Electrical characteristics (operation voltage) of UART0 pins are 1.8 V.

6.1.3 UART1 Pin Interface

Pin Number	Designation	I/O	Description	Electrical Characteristic
61	*UART1_RTS*	Output	UART1 Request to Send (Modem Log port)	1.8 V
65	*UART1_CTS*	Input	UART1 Clear to Send (Modem Log port)	1.8 V
60	*UART1_TX*	Output	UART1 Transmit Data (Modem Log port)	1.8 V
63	*UART1_RX*	Input	UART1 Receive Data (Modem Log port)	1.8 V

Table 25: UART1 Pin Interface

Electrical characteristics (operation voltage) of UART1 pins are 1.8 V.

6.1.4 UART2 Pin Interface

Pin Number	Designation	I/O	Description	Electrical Characteristic
55	*UART2_RTS*	Output	UART2 Request to Send (CLI port)	1.8 V
53	*UART2_CTS*	Input	UART2 Clear to Send (CLI port)	1.8 V
48	*UART2_TX*	Output	UART2 Transmit Data (CLI port)	1.8 V
50	*UART2_RX*	Input	UART2 Receive Data (CLI port)	1.8 V

Table 26: UART2 Pin Interface

Electrical characteristics (operation voltage) of UART2 pins are 1.8 V.

6.1.5 UART0 Host Connection

Connection to host is possible through UART0. This section describes the external host interface which is used to control the modem.

Electrical characteristics (operation voltage) of UART0 pins are 1.8 V.

Below figure shows TX/RX/CTS and RTS connections based on 1.8 V I/O level of external host.

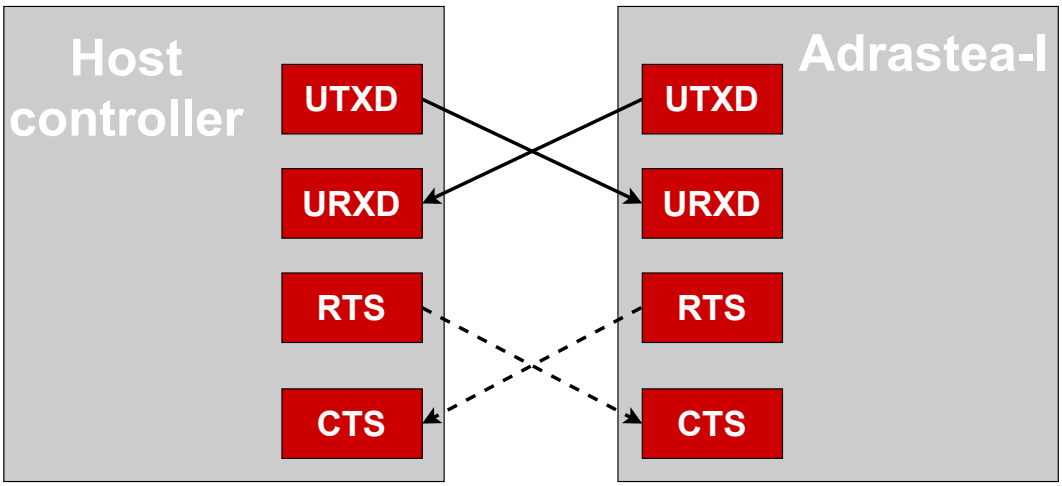


Figure 9: UART0 Host Interface

6.2 SPI Interface

The SPI interface is available when using a customized firmware. It is not implemented within the Adrastea-I default MCU firmware.

6.2.1 SPIM Pin Interface

Electrical characteristics (operation voltage) of SPIM pins are 1.8 V.

Pin Number	Designation	Description	Typ.	Unit
83	*SPIM_MOSI*	SPIM_MOSI connect to SPI Slave SDI	1.8	V
74	*SPIM_MISO*	SPIM_MISO connect to SPI Slave SDO	1.8	V
76	*SPIM_CLK*	SPIM_CLK connect to SPI Slave CLK	1.8	V
81	*SPIM_EN*	SPIM_EN connect to SPI Slave CS	1.8	V

Table 27: SPIM Pin Interface

6.2.2 SPIM Connection

Electrical characteristics (operation voltage) of SPIM pins are 1.8 V.

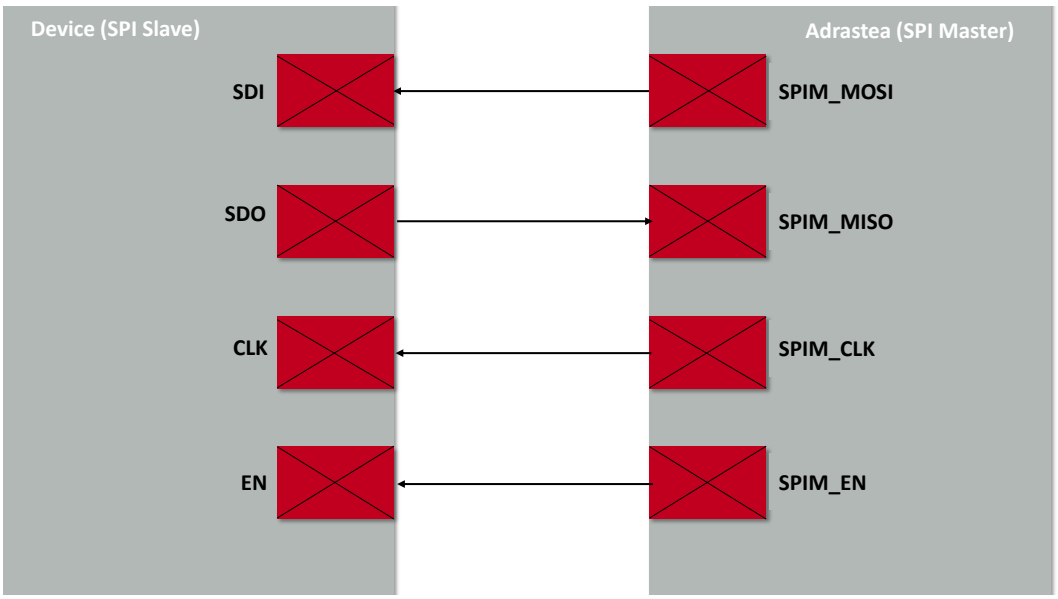


Figure 10: SPIM Connection

6.3 I²C Interface

Adrastea-I provides an I²C interface with clock rate up to 400 kbps. Its operation voltage is 1.8 V.

This interface is enabled but connecting to the external device is subjected to a customized firmware and not supported by the default firmware.

6.3.1 I²C Pin Interface

Electrical characteristics (operation voltage) of I²C pins are 1.8 V.

Pin Number	Designation	Description	Typ.	Unit
15	*I2C_SCL*	I²C SCL connect to external device SCL	1.8	V
17	*I2C_SDA*	I²C SDA connect to external device SDA	1.8	V

Table 28: I²C Pin Interface

6.3.2 I²C Connection

Electrical characteristics (operation voltage) of I²C pins are 1.8 V.

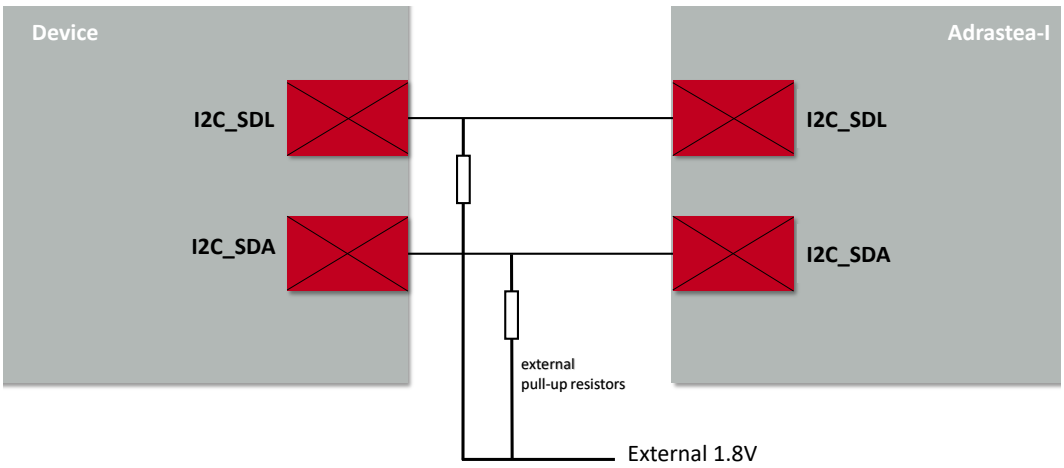


Figure 11: I²C Connection

6.4 ADC Interface

Adrastea-I includes two auxiliary A/D converters to sense external analog inputs.

Electrical characteristics (operation voltage) of ADC pins are 1.8 V.

ADC Interface	Description	Min	Max.	Unit
ADC0	Auxiliary Analog to digital converter channel 0	0	1.8	V
ADC1	Auxiliary Analog to digital converter channel 1	0	1.8	V

Table 29: ADC Interfaces

6.4.1 ADC Functional Specifications

Symbol	Parameter	Min	Typ.	Max	Unit
N	Resolution	6		12	Bits
F_{CLK}	Clock rate	4	40	52	MHz
F_S	Conversion rate per channel (Note1)		F_c /(N+3)		MSPS
V_{IN}	Input voltage range		1.8		V
INL	Integral Nonlinearity		± 1	± 2	LSB
DNL	Differential Nonlinearity	-0.9		0.9	LSB
R_{IN}	Input resistance (Note3)			1.42	MΩ
C_{IN}	Input capacitance during sampling	2.6			pF

Table 30: ADC Functional Specifications

Note1: The general formula for this conversion rate is: F_S=F_{CLK} /(N+3)/Number of sources.
Note2: Conversion rate at 3.46 MSPS and 12bit resolution.
Note3: Measured Input resistance and current on ADC0 with different voltage labels are as below:

Input Voltage (V)	Input Resistance (MΩ)	Measured Current (µA)
1.0	0.98	1.02
1.5	1.42	1.07
1.7	1.38	1.23

Table 31: Measured Input Resistance

6.4.2 ADC Pin Interface

Pin Number	Designation	Description
56	*ADC1/GPIO2*	Auxiliary Analog to Digital Converter Input /Programmable GPIO
59	*ADC0/GPIO1*	Auxiliary Analog to Digital Converter Input /Programmable GPIO

Table 32: ADC Pin Interface

6.5 SIM Interface

Adrastea-I supports 1.8 V SIM cards. SIM card interface follows the ISO 7816 standard.

6.5.1 SIM Pin Interface

Electrical characteristics (operation voltage) of SIM pins are 1.8 V.

Pin Number	Designation	Description
72	*VSIM*	SIM Output voltage
75	*SIMCLK*	SIM Clock
77	*SIMRST*	SIM Reset
79	*SIMIO*	SIM Data

Table 33: SIM Pin Interface

6.6 RF interfaces

Pin Number	Designation	Description
39	*RF_LTE*	RF Signal LTE (The impedance (S11) should be close to 50 Ω, VSWR < 1.5 Refer to our hardware layout recommendations (chapter 9).
43	*RF_GNSS*	RF Signal GNSS (The impedance (S11) should be close to 50 Ω, VSWR < 1.5 Refer to our hardware layout recommendations (chapter 9).

Table 34: RF Pin Interface

6.7 E-JTAG Debug port

The Adrastea-I supports an E-JTAG interface for MCU debugging.

The E-JTAG interface includes the following pins:

Pin Number	Designation	Description
10	*EJ_TCK*	JTAG Test Clock
12	*EJ_TDO*	JTAG Test Data Output
14	*EJ_TDI*	JTAG Test Data Input
16	*EJ_TMS*	JTAG Test Mode Select
18	*EJ_TRST*	JTAG Test Reset (Required external Pull down)
84	*DEBUG_SEL*	HW Pin for EJTAG chain selection

Table 35: E-JTAG Debug port

These pins are not multiplexed with other interfaces in order to save them for debug purposes. The debug port can be directed in direct line to the modem debug chain or MCU.The default direction is set according to the external pin state (DEBUG_SEL). The DEBUG_SEL has an internal Pull Down by default.

Adrastea-I has an internal PD for EJ_TRST, as it is a very sensitive line (in case it will toggle high the processor will enter debug mode), we suggest not keeping it unconnected but to connect it to an external 10K ohm PD. Other E-JTAG pins can be kept NC.

6.8 GPIO Pin Information

Pin Number	Designation	Description
56	*ADC1/GPIO2*	Auxiliary Analog to Digital Converter Input /Programmable GPIO Default pull resistor at power up and after DH0: Pull Down DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
59	*ADC0/GPIO1*	Auxiliary Analog to Digital Converter Input /Programmable GPIO Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
66	*RESERVED*	Reserved /Programmable GPIO49 Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
68	*RESERVED*	Reserved /Programmable GPIO46 Default pull resistor at power up and after DH0: Pull Down DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
71	*RESERVED*	Reserved /Programmable GPIO48 Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull

73	*RESERVED*	Reserved /Programmable GPIO47 Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
74	*SPIM1_MISO/GPIO39*	MCU_SPIM1_MISO/Programmable GPIO Default pull resistor at power up and after DH0: Pull Down DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
76	*SPIM1_CLK/GPIO41*	MCU_SPIM1_CLK/Programmable GPIO Default pull resistor at power up and after DH0: Pull Down DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
81	*SPIM1_EN/GPIO40*	MCU SPI Enable/Programmable GPIO Default pull resistor at power up and after DH0: Pull Up DH2 state: SW configurable DH1 state: No pull DH0 state: No pull
83	*SPIM1_MOSI/GPIO38*	MCU_SPIM1_MOSI/Programmable GPIO Default pull resistor at power up and after DH0: Pull Down DH2 state: SW configurable DH1 state: No pull DH0 state: No pull

Table 36: GPIO Pin Information

These GPIO pins are available when using a customized MCU firmware. These are not implemented within the Adrastea-I default MCU firmware.

1. SW can configure these pins in different state for DH2.
2. There is ESD protector in ALT1250. During DH0/DH1, it should not have any PU externally to avoid current leakage.

7 Functional description

The Adrastea-I LTE-M/NB-IoT module is intended to be used as a radio sub-system in order to provide LTE-M/NB-IoT communication capabilities to the system.

The Adrastea-I modem firmware is 3GPP Release 13 compliant, which is upgradable to Release-14.

The UART-0 acts as the primary interface between the module and a host micro-controller. The module can be controlled and operated using a set of AT-commands over UART-0.

Adrastea-I is a high-performance, multi-band dual mode LTE-M/NB-IoT module with ultra-low power consumption.

Embedded GNSS allows location applications to track positioning.

7.1 Adrastea-I State Transition

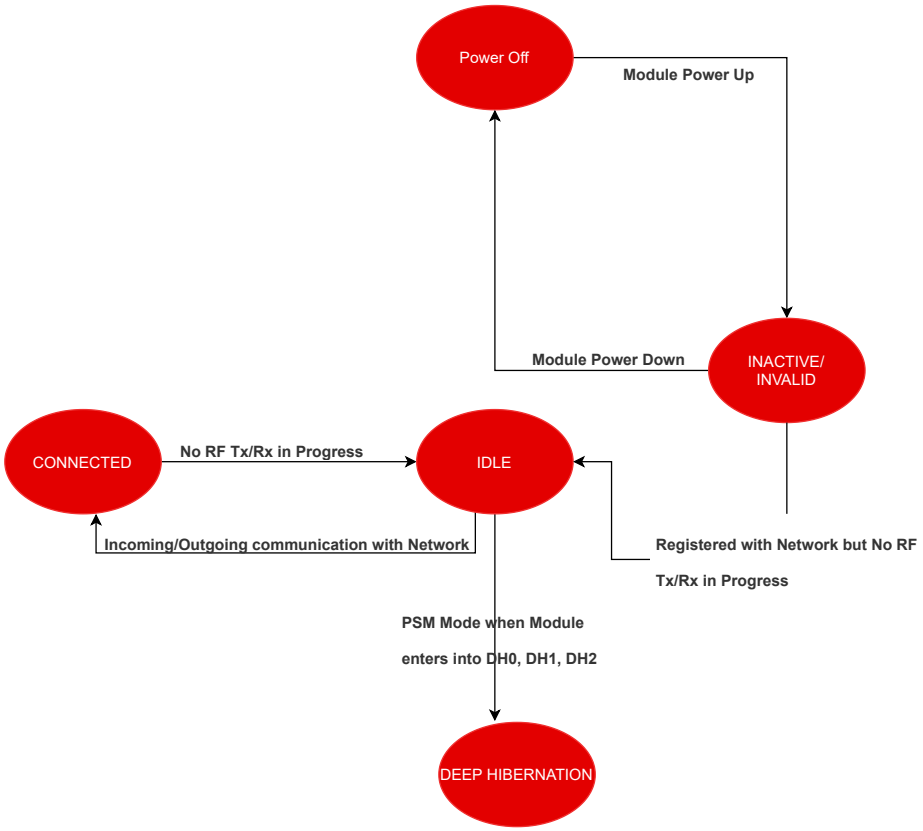


Figure 12: Adrastea-I State Transition

7.2 Power Saving Features

To enhance the battery life of cellular IoT devices, 3GPP has introduced two key technologies: Extended Discontinuous Reception (eDRX) and Power Saving Mode (PSM). These technologies allow devices to enter into low-power states when not actively transmitting data, significantly reducing power consumption.

7.3 Network Operator Support

For the Adrastea-I module to operate correctly in eDRX and PSM modes, these features must be enabled by the network operator. However, eDRX and PSM configurations can vary between operators, and some may not support these features. This variability can impact the power-saving capabilities of the Adrastea-I.

7.4 Network Independent Adrastea-I Power Saving Modes

To ensure optimal power savings regardless of network operator support, it is recommended to use the Adrastea-I module's power-saving modes independently. This can be achieved by disabling the LTE RF of the device using the AT+CFUN=0 command. This approach allows you to benefit from power-saving features of the module independent of network.

This section summarizes the various low power operating modes of the Adrastea-I module.

The Adrastea-I selects the described power modes according to the the maximum allowed chip power mode configuration. The currently configured power mode can be checked with AT command:
at%getacfg="pm.conf.max_allowed_pm_mode"

7.4.1 DH0 Mode

DH0 mode provides long entry and recovery times and is mainly used for very long inactivity intervals like power saving mode. In this mode all digital logic is powered down, memories are not retained, I/O are not stored.

This is the lowest power mode of the system.

One of the following dedicated actions is used to wake up from this mode:

- WAKEUP (Wakeup active high).
- Module reset (/RESET - Reset active low).
- Module power down.

In this mode VDDIO is turned off, therefore it is not allowed to provide external voltage to IOs that are not defined as a wake up source in the list above.

When Adrastea-I enters the DH0 state, it writes data to the flash memory. To prevent flash wear out, ALT1250 chip has implemented a flash wear out protection feature. This feature prevents the module from entering DH0 mode if less than 30 minutes have passed since the last DH0 mode or if less than 30 minutes of DH0 sleep is expected. In such cases, the module will enter into DH1 state instead of DH0.

7.4.2 DH1 Mode

All digital logic is powered down, a configurable amount of retention memory is retained (64KB granularity), IOs are not stored.

One of the following dedicated actions is used to wake up from this mode:

- WAKEUP (Wakeup active high).
- Module reset (/RESET - Reset active low).
- Module power down.

A Wakeup event initiates a boot flow. This mode is similar to DH2; however, lower power consumption due to I/O logic unretained.

In this mode VDDIO is turned off, therefore it is not allowed to provide external voltage to IOs that are not defined as a wake up source in the list above.

7.4.3 DH2 Mode

Achieve the lowest power consumption while retaining the content of SRAM and registers. All digital logic is powered down.
One of the following dedicated pins is used to wake up from this mode:

- WAKEUP (Wakeup active high).
- Module reset (/RESET - Reset active low).
- Module power down.

Wakeup event initiates a boot flow. This mode is similar to DH1; however, it also enables output IOs to latch and wakeup from digital inputs.

Adrastea-I is set by default in DH2 state.

7.4.4 DH0 Mode Setting

1. Check whether the DH0 state is configured

```
at%getacfg="pm.conf.max_allowed_pm_mode"
dh0

OK
```

2. If the DH0 state is not already configured, configure the module to DH0 state with below AT command.

```
AT+CFUN=0

OK

at%setacfg="pm.conf.max_allowed_pm_mode","dh0"

OK
```

3. Reset the Adrastea-I.

```
ATZ

OK
```

4. Turn off the RF with the below AT command. This approach allows you to benefit from power-saving feature of the module independent of network.

```
AT+CFUN=0

OK
```

5. Enter "CTRL+D" to close the CLI.

```
CTRL+D

MAP CLI Closed
```

To execute below commands default MCU firmware "PowerManager" shall be present in MCU.

6. The "pwrMode shutdown" command is used to configure MCU in shutdown state.

```
>>pwrMode shutdown

Configured to Shutdown mode, duration 0ms
```

7. The "sleepSet enable" command is used to enable MCU shutdown state.

```
>>sleepSet enable

Configured to Shutdown mode, duration 0ms
```

After following the above steps, the Adrastea-I module will now be in DH0 state and the MCU is shutdown.

When Adrastea-I enters the DH0 state, it writes data to the flash memory. To prevent flash wear out, ALT1250 chip has implemented a flash wear out protection feature. This feature prevents the module from entering DH0 mode if less than 30 minutes have passed since the last DH0 mode or if less than 30 minutes of DH0 sleep is expected. In such cases, the module will enter into DH1 state instead of DH0.

7.4.5 DH1 Mode Setting

1. Check whether the DH1 state is configured

```
at%getacfg="pm.conf.max_allowed_pm_mode"
dh1
```

```
OK
```

2. If the DH1 state is not already configured, configure the module to DH1 state with below AT command.

```
AT+CFUN=0

OK

at%setacfg="pm.conf.max_allowed_pm_mode","dh1"

OK
```

3. Reset the Adrastea-I.

```
ATZ

OK
```

4. Turn off the RF with the below AT command. This approach allows you to benefit from power-saving feature of the module independent of network.

```
AT+CFUN=0

OK
```

5. Enter "CTRL+D" to close the CLI.

```
CTRL+D

MAP CLI Closed
```

To execute below commands default MCU firmware "PowerManager" shall be present in MCU.

6. The "pwrMode shutdown" command is used to configure MCU in shutdown state.

```
>>pwrMode shutdown

Configured to Shutdown mode, duration 0ms
```

7. The "sleepSet enable" command is used to enable MCU shutdown state.

```
>>sleepSet enable

Configured to Shutdown mode, duration 0ms
```

After following the above steps, the Adrastea-I module will now be in DH1 state and the MCU is shutdown.

7.4.6 DH2 Mode Setting

1. Check whether the DH2 state is configured

```
at%getacfg="pm.conf.max_allowed_pm_mode"
dh2


OK
```

2. If the DH2 state is not already configured, configure the module to DH2 state with the below AT command.

```
AT+CFUN=0

OK

at%setacfg="pm.conf.max_allowed_pm_mode","dh2"

OK
```

3. Reset the Adrastea-I.

```
ATZ
```

```
OK
```

4. Turn off the RF with the below AT command. This approach allows you to benefit from power-saving feature of the module independent of network.

```
AT+CFUN=0

OK
```

5. Enter "CTRL+D" to close the CLI.

```
CTRL+D

MAP CLI Closed
```

To execute below commands default MCU firmware "PowerManager" shall be present in MCU.

6. The "pwrMode shutdown" command is used to configure the MCU in shutdown state.

```
>>pwrMode shutdown

Configured to Shutdown mode, duration 0ms
```

7. The "sleepSet enable" command is used to enable the MCU shutdown state.

```
>>sleepSet enable

Configured to Shutdown mode, duration 0ms
```

After following the above steps, the Adrastea-I module will be in DH2 state and the MCU is shutdown.

7.5 GNSS Receiver

Adrastea-I supports GPS and GLONASS satellite systems using dedicated hardware accelerators in a power and cost efficient manner. The GNSS receiver shares certain hardware resources with the modem. This enables GNSS measurement slots to be efficiently scheduled based on the modem link state. The device key target is to allow GNSS positioning for asset management applications where infrequent position updates are required. External LTE and GNSS antennas are required.

7.5.1 Supported GNSS constellations

Adrastea-I supports the following constellation combinations:

- GPS
- GLONASS

7.5.2 GNSS Co-existence with LTE Modem

The Adrastea-I GNSS shares the RF Rx path with the LTE modem and, therefore, cannot operate in parallel with LTE data transfer. Hence this GNSS is not suitable for products that inherently require this co-existence, LTE connection and GNSS tracking.

GNSS cannot co-exist with LTE data transfer. LTE communication has higher priority over GNSS and, therefore, GNSS is automatically shut down once LTE is active (if it was active). While LTE is active, GNSS cannot be activated and all GNSS AT commands are responded with error.

7.6 Application MCU

Effective January 1, 2026, Sony will discontinue support for Open MCU for all new designs based on the ALT1250 chipset. As a result, using the integrated Arm Cortex M4 MCU of Adrastea-I for new application development is not recommended. However, using Adrastea-I as a modem is not affected by this announcement.

8 Quick start guide

It is recommended to use the Adrastea-I EV-Kit and Adrastea Commander tool for putting the LTE-M/NB-IoT module into operation. The EV-Kit has external GNSS and LTE antennas. Refer to the [2] for detailed information.

8.1 Minimal pin connections

The following image shows the steps to be performed to integrate the Adrastea-I into a custom end device.

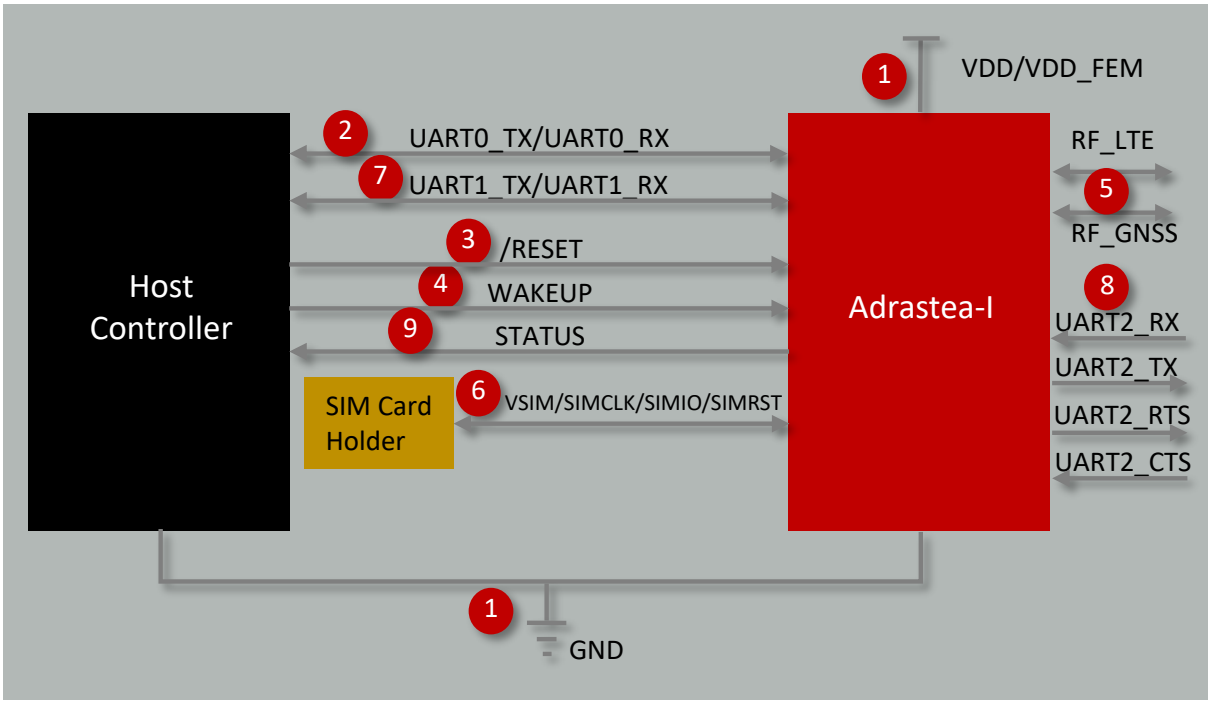


Figure 13: Minimal pin connections

1. Supply voltage and ground
   Connect the *VDD*, *VDD_FEM* and *GND* pins to supply the radio module with power.

Note the minimum voltage acceptance difference between *VDD* and *VDD_FEM*.

2. MCU UART0 serial interface to the host
   Connect the UART pins *UART0_RX* and *UART0_TX* to the host to control the module via host controller.

3. Reset
   Connect the */RESET* pin to the host to allow a hard reset of the module.

4. Wakeup
   Connect the *WAKEUP* pin to the host to allow the waking-up function of the module.
5. Antenna connection
   Connect the *RF_LTE* pin to an external LTE antenna. Connect the *RF_GNSS* pin to an external GNSS antenna.
6. SIM card connection
   Connect the followings pins to a proper SIM card holder to allow network connection: *VSIM*, *SIMCLK*, *SIMIO* and *SIMRST*.
7. (Optional) MCU UART1 serial interface for modem logs
   Connect the UART pins *UART1_RX* and *UART1_TX* to obtain modem logs.
8. (Optional) MCU UART2 serial interface for firmware update
   Connect the UART pins *UART2_RX*, *UART2_TX*, *UART2_CTS* and *UART2_RTS* to execute firmware updates.
9. (Optional) Status indication
   Connect the *STATUS* pin to the host controller to allow easy indication of the status.

The logic level of the module is based on 1.8 V. A 3.3 V. Logic level shall not be connected directly to the digital interfaces of the module

If the module has to be connected to a PC, a converter (TTL to RS-232 or TTL to USB) has to be used. See chapter `Pinout` for details on all pins. Refer to the Adrastea-I EV-Board schemes for a `Reference design`.

8.2 Prerequisites

1. Adrastea-I EV-Kit.
2. Computer with a serial terminal emulator. The use of Würth Elektronik eiSos's Adrastea Commander is recommended ([1]).
3. Install on your PC the corresponding FTDI driver package. Click on link 1 (FTDI drivers) in the "Adrastea Commander" tool or download direct from *https://www.ftdichip.com/Drivers/VCP.htm*.
4. A valid NB-IoT and LTE-M enabled nano SIM card.

The Adrastea-I EV-Board comes with a nano SIM card holder. Therefore, we recommend using a nano SIM card in this step. When designing a custom application board, users may choose to implement a SIM card holder of any size (nano, micro, or standard) according to their specific design requirements that meet SIM card interface as described in `SIM Interface`

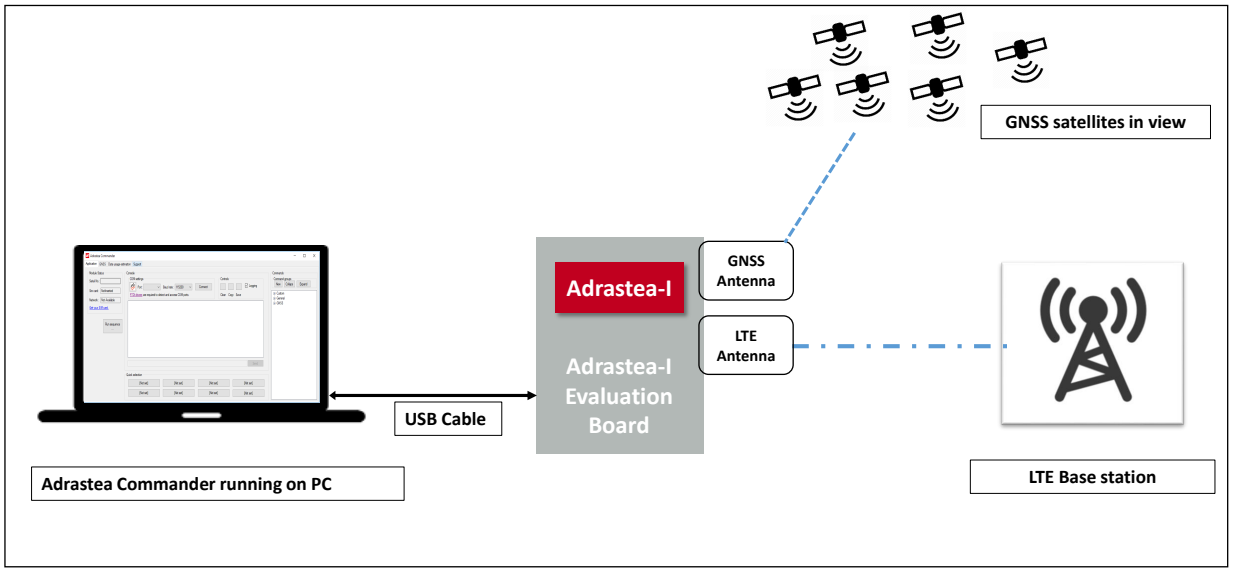


Figure 14: Adrastea Commander

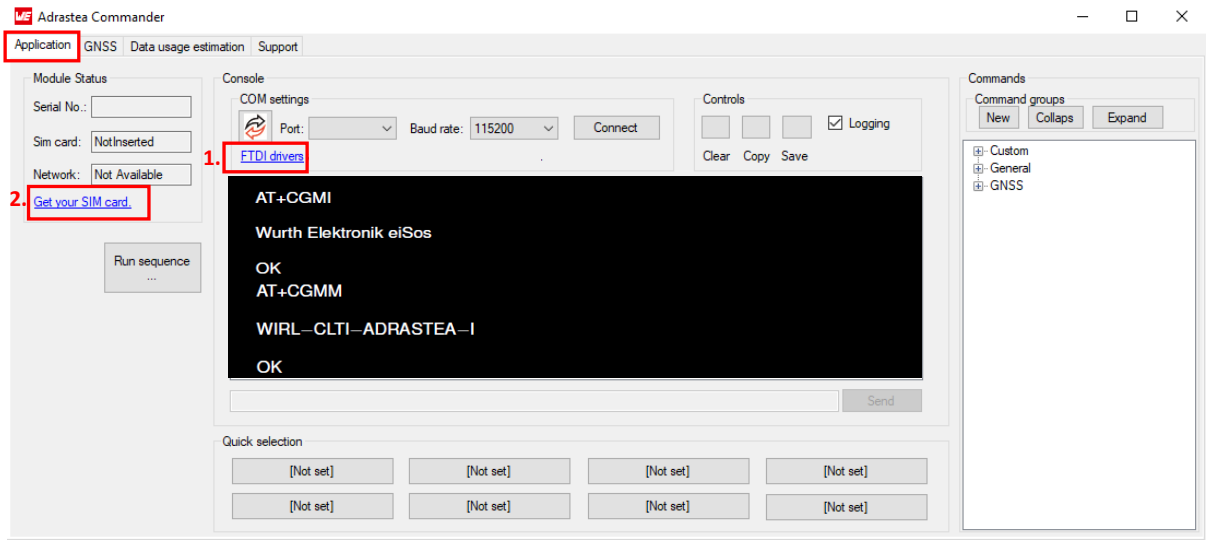


Figure 15: Adrastea Commander

8.3 Taking into operation

1. Insert a valid NB-IoT and LTE-M enabled nano SIM card.
2. Connect LTE and GNSS external antennas provided with the EV-Kit.
3. Connect the power jack or external power supply to the EV-Board and verify that the VDD is stable and able to reliably supply the module's static and peak current consumption, as specified in the data sheet and user manual.
4. Connect the EV-Board to the PC using a USB-cable. Four COM ports should be detected and installed on your PC. Check the device manager to acquire the COM port names of the EV-Board. A typical name is "COMxy" in Windows systems or /dev/ttyUSB0 in Linux systems.

Note that usually the four COM ports are assigned in ascending order, as shown in figure 16. However, the exact sequence may vary depending on your operating system.

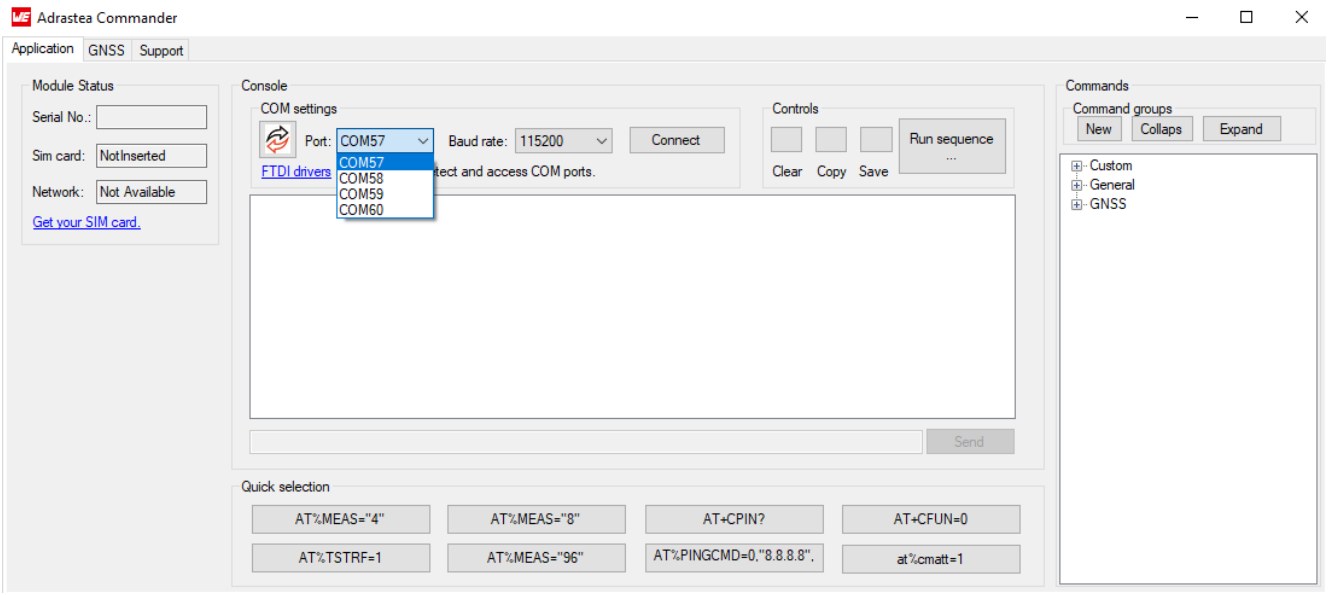


Figure 16: COM ports detected - Adrastea commander

To interact with the module, it is advised to use the Adrastea Commander tool. Otherwise, a terminal program (like "PuTTY" or "Tera Term" for Windows) has to be run and the corresponding COM port has to be opened using the default settings of the mounted Adrastea-I module.

5. Press the reset button on the EV-Board to ensure a clean start-up of the module. See figure 17.
6. Type and enter the "map" command, this command is required before sending AT commands to modem.

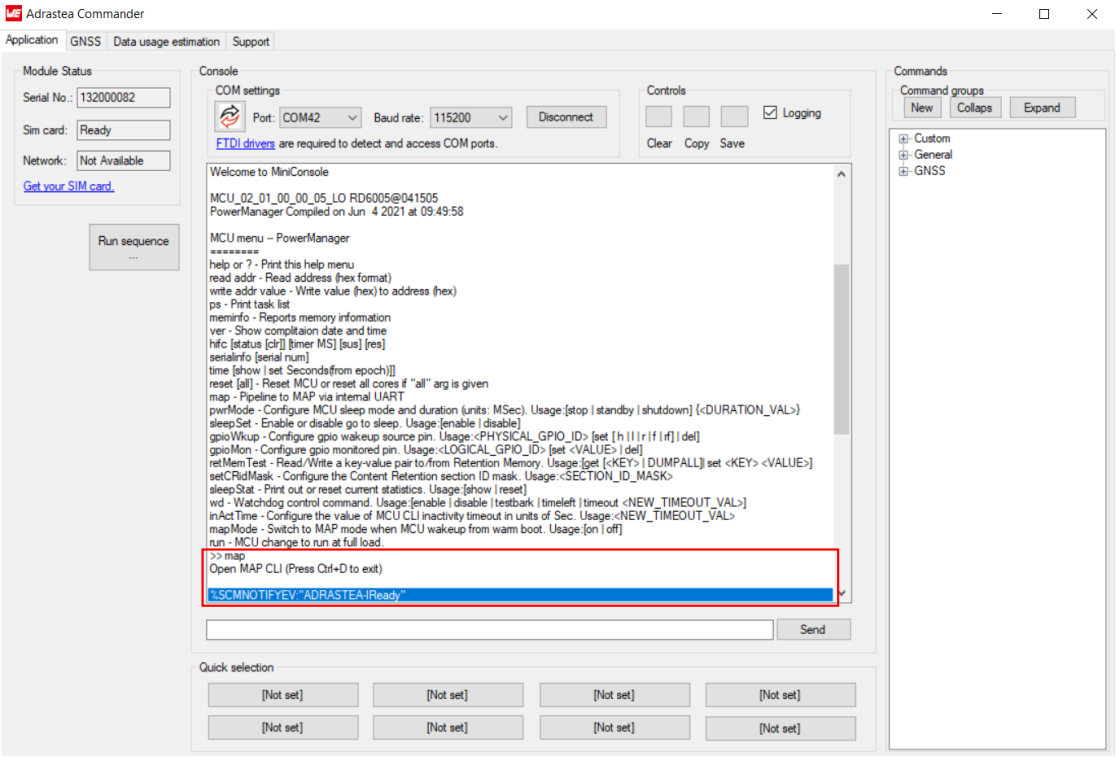


Figure 17: MiniConsole start view - Adrastea Commander

The "map" command is required before sending AT commands to modem.

When the AT Command UART port is opened, the Adrastea-I output console displays: %SCMNOTIFYEV:"ADRASTEA-IReady".

7. Check if the SIM card is detected. Send command `MAP` follow by the command AT+CPIN?. See figure `18`.

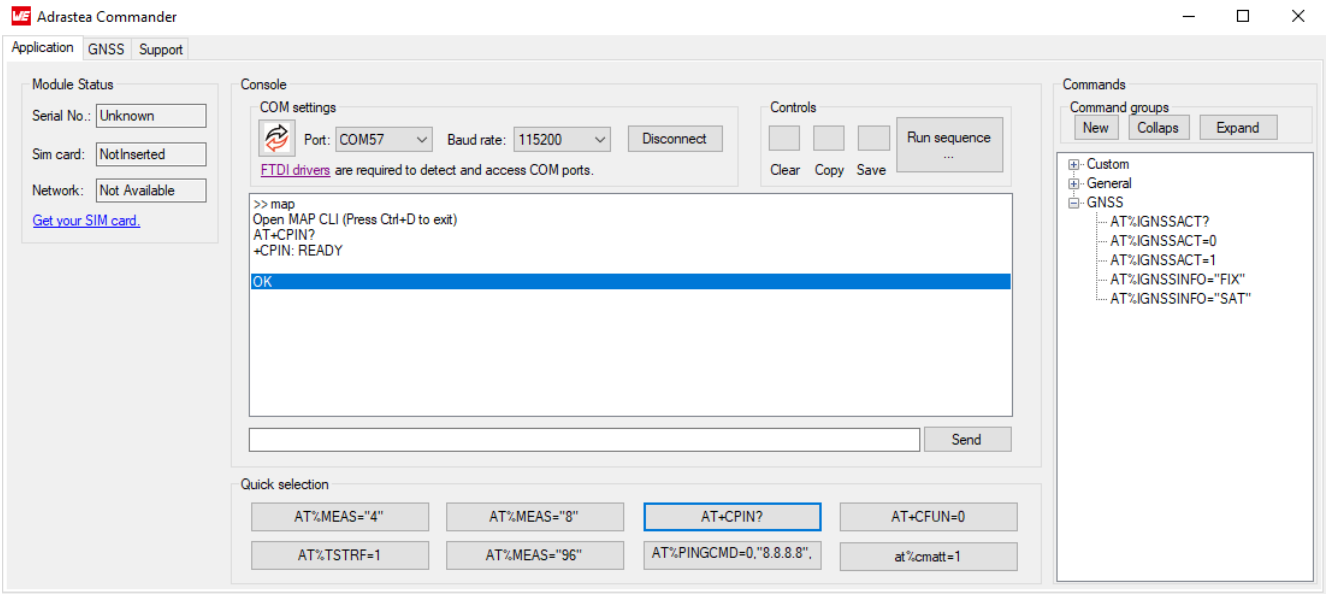


Figure 18: SIM card detected - Adrastea Commander

8.4 Select LTE-M or NB-IoT Mode

Adrastea-I can be operated through one of the two available cellular communication technologies:

- LTE-Cat.M or
- LTE-Cat.NB-IoT.

Two different configurations can be applied for selection of LTE-Cat.M or LTE-Cat.NB-IoT mode.

- Manual selection of LTE-M or NB-IoT mode or
- Automatic selection of LTE-M or LTE-NB-IoT mode

8.4.1 Manual selection of LTE-M or NB-IoT mode

Adrastea-I supports AT commands for manual selection of LTE-M and NB-IoT. AT Command AT%RATACT is used for manual selection of the LTE-M or NB-IoT mode.

Note: The default mode for the Adrastea-I module is LTE-M single mode.

Any attempt to switch to the mode already in use will be ignored and OK will be returned.

1. Select relevant RAT:

   The following AT command will change the module mode to NB-IoT.

```
AT%RATACT="NBIOT",1
OK
```

   The following AT command can be used to verify that NB-IoT has been selected.

```
AT%RATACT?
%RATACT: "NBIOT",1,0
OK
```

   The following AT command will change the module mode to LTE-M.

```
AT%RATACT="CATM",1
OK
```

The following AT command can be used to verify that LTE-M has been selected.

```
AT%RATACT?
%RATACT: "CATM",1,0
OK
```

2. Reset the device:
   The following AT command is used to reset the device.

```
ATZ

OK
```

8.4.2 Automatic Selection of LTE-M or NB-IoT Mode

The automatic selection is used to switch between the LTE-M and NB-IoT when no coverage in the current RAT is detected. RAT switch related configurations are included in the radiom configuration file inside the ALT1250 chipset.

Default configurations of Adrastea-I are as below:

```
at%getacfg=radiom.config.multi_rat_enable
true
OK

at%getacfg=radiom.config.preferred_rat_list
none
OK

at%getacfg=radiom.config.auto_preference_mode
none
OK
```

Configure Adrastea-I as below for automatic selection of LTE-M or NB-IoT mode:

1. Disable LTE radio:

```
AT+CFUN=0

OK
```

2. Enable multi-technologies:

```
at%setacfg="radiom.config.multi_rat_enable","true"

OK
```

3. Set technology priority order for automatic selection. The below command sets the first priority for NB-IoT and the second priority for LTE-M:

```
at%setacfg="radiom.config.preferred_rat_list","NBIOT;CATM"

OK
```

Note: In case of the above configuration, Adrastea-I will scan all the frequencies in the NB-IoT technology first. If Adrastea-I does not find coverage in NB-IoT, it will scan all the frequencies in the LTE-M technology. Because of this frequency scanning process, power consumption in automatic selection process is higher than in manual selection process.

4. The Adrastea-I applies automatic technology switch at the switch-on and in the out-of coverage case:

```
at%setacfg="radiom.config.auto_preference_mode","light"

OK
```

5. Restart the Adrastea-I:

```
ATZ

OK
```

To set default factory configurations follow below commands:

at%setacfg="radiom.config.multi_rat_enable",true

OK

at
OK

at
OK

8.5 Register to Network

The configurations "Select LTE-M or NB-IoT Mode" (see Chapter 8.4) should be done before registering to the LTE network.

A valid LTE-M/NB-IoT SIM card should be inserted. Check SIM status with AT+CPIN? AT Command.

The registration process in LTE-M and NB-IoT technologies could take some minutes to complete. This happens especially in case of the very first registration: new SIM, new location, new module. This is because of scanning of available frequencies and selection of a suitable frequency.

1. Check SIM status:

   The following command is used to read the SIM status.

   ```
   AT+CPIN?

   +CPIN: READY
   OK
   ```

2. To start the registration procedure:

   The following command will trigger the registration procedure with the network.

```
AT%CMATT=1

OK
```

3. Enable network registration unsolicited result code:
   The following command will enable network registration and location information unsolicited result code.

```
AT+CEREG=2

OK
```

4. Read the network registration status:

   The following command will read the network registration status.

```
AT+CEREG?
+CEREG: 2,5,"CB48","01CD6007",9
OK
```

5. Check the internet connection is active, ping google server with IP address 8.8.8.8:

Google server will be reachable only when global APN is configured

```
AT%PINGCMD=0,"8.8.8.8"
%PINGCMD:1,"8.8.8.8",1042,58

OK
```

The following command will trigger the de-registration procedure with the network.

```
AT%CMATT=0

OK
```

8.6 Activate GNSS

This section shows how to enable the GNSS feature of the Adrastea-I module.

GNSS cannot co-exist with LTE data transfer. LTE communication has higher priority over GNSS and, therefore, GNSS is automatically shut down once LTE is active (if it was active). While LTE is active, GNSS cannot be activated and all GNSS AT commands are responded with error.

1. Disable LTE prior to activating GNSS:

   The following command will disable LTE radio.

```
AT+CFUN=0

OK
```

2. Allow unsolicited notifications:

```
AT%IGNSSEV="SESSIONSTAT",1

OK
```

3. Enable NMEA sentences (This command is required only when messages are required in GNSS tab of Adrastea Commander tool):

```
AT%IGNSSCFG="SET","NMEA","GGA","GSA","GSV","GNS","RMC"

OK
```

4. Start GNSS:

For first time GNSS fix, cold start should be triggered to start GNSS.

The following command is used for cold GNSS start.

```
AT%IGNSSACT=1,1

OK
```

The following command is used for hot GNSS Start.

```
AT%IGNSSACT=1,2

OK
```

5. Get available satellites:

It is necessary to check that there are at least 4 satellites available with an SNR>25.

```
AT%IGNSSINFO="SAT"
%IGNSSINFO: 11
%IGNSSINFO:03,36,294,49
%IGNSSINFO:06,53,263,50
%IGNSSINFO:14,42,180,50
%IGNSSINFO:15,13,042,50
%IGNSSINFO:16,08,251,50
%IGNSSINFO:18,56,044,50
%IGNSSINFO:19,25,314,50
%IGNSSINFO:21,46,104,51
%IGNSSINFO:22,71,306,49
%IGNSSINFO:24,14,080,49
%IGNSSINFO:27,51,282,50
```

6. Get fix:

```
AT%IGNSSINFO="FIX"

%IGNSSINFO: 2,"11:17:02","04/05/2020","32.195970","34.892572","
    −10.500000",1588580222000,1,"0.000000","B"
```

The following AT command is used to stop GNSS functionality:

```
AT%IGNSSACT=0

OK
```

9 Design in guide

9.1 Advice for schematic and layout

For users with less RF experience it is advisable to closely copy the relating EV-Board with respect to schematic and layout, as it is a proven design. The layout should be conducted with particular care, because even small deficiencies could affect the radio performance and its range or even the conformity.
The following general advice should be taken into consideration:

- A clean, stable power supply is strongly recommended. Interference, especially oscillation can severely restrain range and conformity.
- Variations in voltage level should be avoided.
- LDOs, properly designed in, usually deliver a proper regulated voltage.
- Blocking capacitors and a ferrite bead in the power supply line can be included to filter and smoothen the supply voltage when necessary.

No fixed values can be recommended, as these depend on the circumstances of the application (main power source, interferences etc.).

The use of an external reset IC should be considered if one of the following points is relevant:

- The slew rate of the power supply exceeds the electrical specifications.
- The effect of different current consumptions on the voltage level of batteries or voltage regulators should be considered. The module draws higher currents in certain scenarios like start-up or radio transmit which may lead to a voltage drop on the supply. A restart under such circumstances should be prevented by ensuring that the supply voltage does not drop below the minimum specifications.
- Voltage levels below the minimum recommended voltage level may lead to malfunction. The /Reset pin of the module shall be held on LOW logic level whenever the VCC is not stable or below the minimum operating Voltage.
- Special care must be taken in case of battery powered systems.

- Elements for ESD protection should be placed on all pins that are accessible from the outside and should be placed close to the accessible area. For example, the RF-pin is accessible when using an external antenna and should be protected.
- ESD protection for the antenna connection must be chosen such as to have a minimum effect on the RF signal. For example, a protection diode with low capacitance such as the 8231706A or a 68 nH air-core coil connecting the RF-line to ground give good results.
- Placeholders for optional antenna matching or additional filtering are recommended.
- The antenna path should be kept as short as possible.

Again, no fixed values can be recommended, as they depend on the influencing circumstances of the application (antenna, interferences etc.).

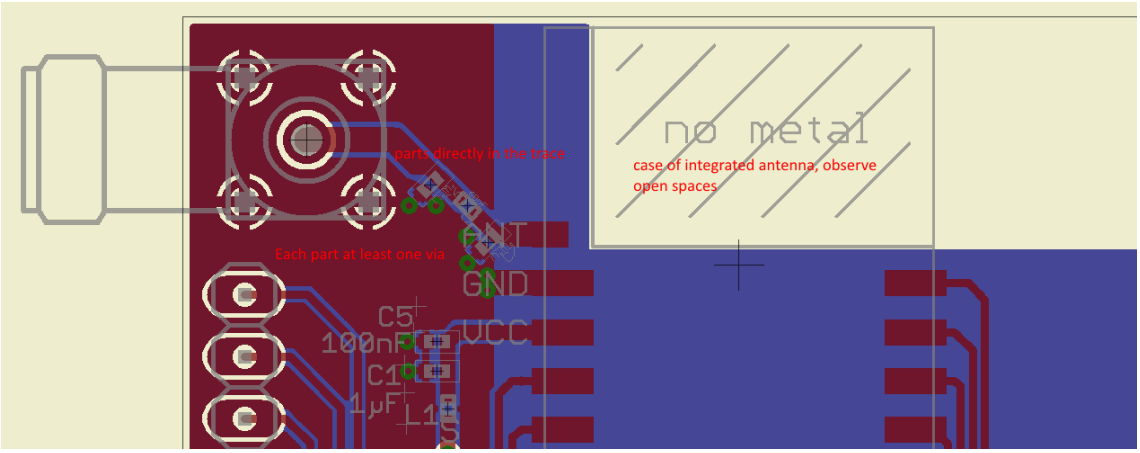


Figure 19: Layout

- To avoid the risk of short circuits and interference there should be only the necessary routing underneath the module on the top layer of the baseboard.
- On the second layer, a ground plane is recommended, to provide good grounding and shielding to any following layers and application environment.
- Filter and blocking capacitors should be placed directly in the tracks without stubs, to achieve the best effect.
- Antenna matching elements should be placed close to the antenna / connector, blocking capacitors close to the module.
- Ground connections for the module and the capacitors should be kept as short as possible and with at least one separate through hole connection to the ground layer.
- ESD protection elements should be placed as close as possible to the exposed areas.

9.2 Dimensioning of the micro strip antenna line

The antenna track has to be designed as a 50 Ω feed line. The width W for a micro strip can

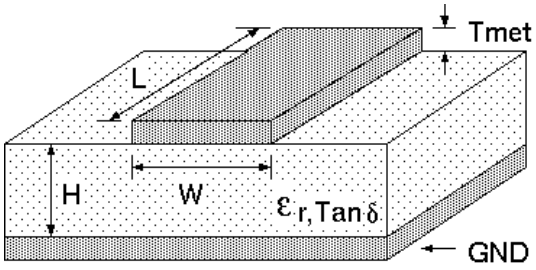


Figure 20: Dimensioning the antenna feed line as micro strip

be calculated using the following equation:

$$W = 1.25 \times \left(\frac{5.98 \times H}{e^{\frac{50 \times \sqrt{\epsilon_r} + 1.41}{87}}} - T_{met} \right) \quad (1)$$

Example:
A FR4 material with ε_r = 4.3, a height H = 1000 µm and a copper thickness of T_{met} = 18 µm will lead to a trace width of W ~ 1.9 mm. To ease the calculation of the micro strip line (or e.g. a coplanar) many calculators can be found in the internet.

- As rule of thumb a distance of about 3×W should be observed between the micro strip and other traces / ground.
- The micro strip refers to ground, therefore there has to be the ground plane underneath the trace.
- Keep the feeding line as short as possible.

9.3 Antenna solutions

There exist several kinds of antennas, which are optimized for different needs. Chip antennas are optimized for minimal size requirements but at the expense of range, PCB antennas are optimized for minimal costs, and are generally a compromise between size and range. Both usually fit inside a housing.
Range optimization in general is at the expense of space. Antennas that are bigger in size, so that they would probably not fit in a small housing, are usually equipped with a RF connector. A benefit of this connector may be to use it to lead the RF signal through a metal plate (e.g. metal housing, cabinet).
As a rule of thumb a minimum distance of λ /10 (which is 3.5 cm @ 868 MHz and 1.2 cm @ 2.44 GHz) from the antenna to any other metal should be kept. Metal placed further away will not directly influence the behavior of the antenna, but will anyway produce shadowing.

Keep the antenna as far as possible from large metal objects to avoid electromagnetic field blocking.

The choice of antenna might have influence on the safety requirements.

In the following chapters, some special types of antenna are described.

9.3.1 Wire antenna

An effective antenna is a λ /4 radiator with a suiting ground plane. The simplest realization is a piece of wire. It's length is depending on the used radio frequency, so for example 8.6 cm 868.0 MHz and 3.1 cm for 2.440 GHz as frequency. This radiator needs a ground plane at its feeding point. Ideally, it is placed vertically in the middle of the ground plane. As this is often not possible because of space requirements, a suitable compromise is to bend the wire away from the PCB respective to the ground plane. The λ/4 radiator has approximately 40 Ω input impedance. Therefore, matching is not required.

9.3.2 Chip antenna

There are many chip antennas from various manufacturers. The benefit of a chip antenna is obviously the minimal space required and reasonable costs. However, this is often at the expense of range. For the chip antennas, reference designs should be followed as closely as possible, because only in this constellation can the stated performance be achieved.

9.3.3 PCB antenna

PCB antenna designs can be very different. The special attention can be on the miniaturization or on the performance. The benefits of the PCB antenna are their small / not existing (if PCB space is available) costs, however the evaluation of a PCB antenna holds more risk of failure than the use of a finished antenna. Most PCB antenna designs are a compromise of range and space between chip antennas and connector antennas.

9.3.4 Antennas provided by Würth Elektronik eiSos

Besides the radio modules Würth Elektronik eiSos provides various antennas tailored for the different frequency bands. The recommended single external antennas are shown in the subsequent chapters.

In case integrated multilayer chip antennas are needed because of space limitations, please refer to
https://www.we-online.com/en/components/products/WE-MCA.

9.3.4.1 2600130084 - Hati-I - LTE antenna

Figure 21: Hati-I antenna

Specification	Value
Frequency range [MHz]	700 – 2700
Impedance [Ω]	50
VSWR	$\leq$ 3 / 3.5
Polarization	Linear
Gain [dBi]	3.3 / 6
Dimensions [mm]	157 x 6 x 21
Connector	SMA male
Operating Temp. [°C]	-40 – +85

10 Reference design

Adrastea-I was tested on the EV-Board which serves as reference design.
Further information concerning the use of the EV-Board can be found in the manual of the Adrastea-I EV-Board [2].

10.1 Schematic

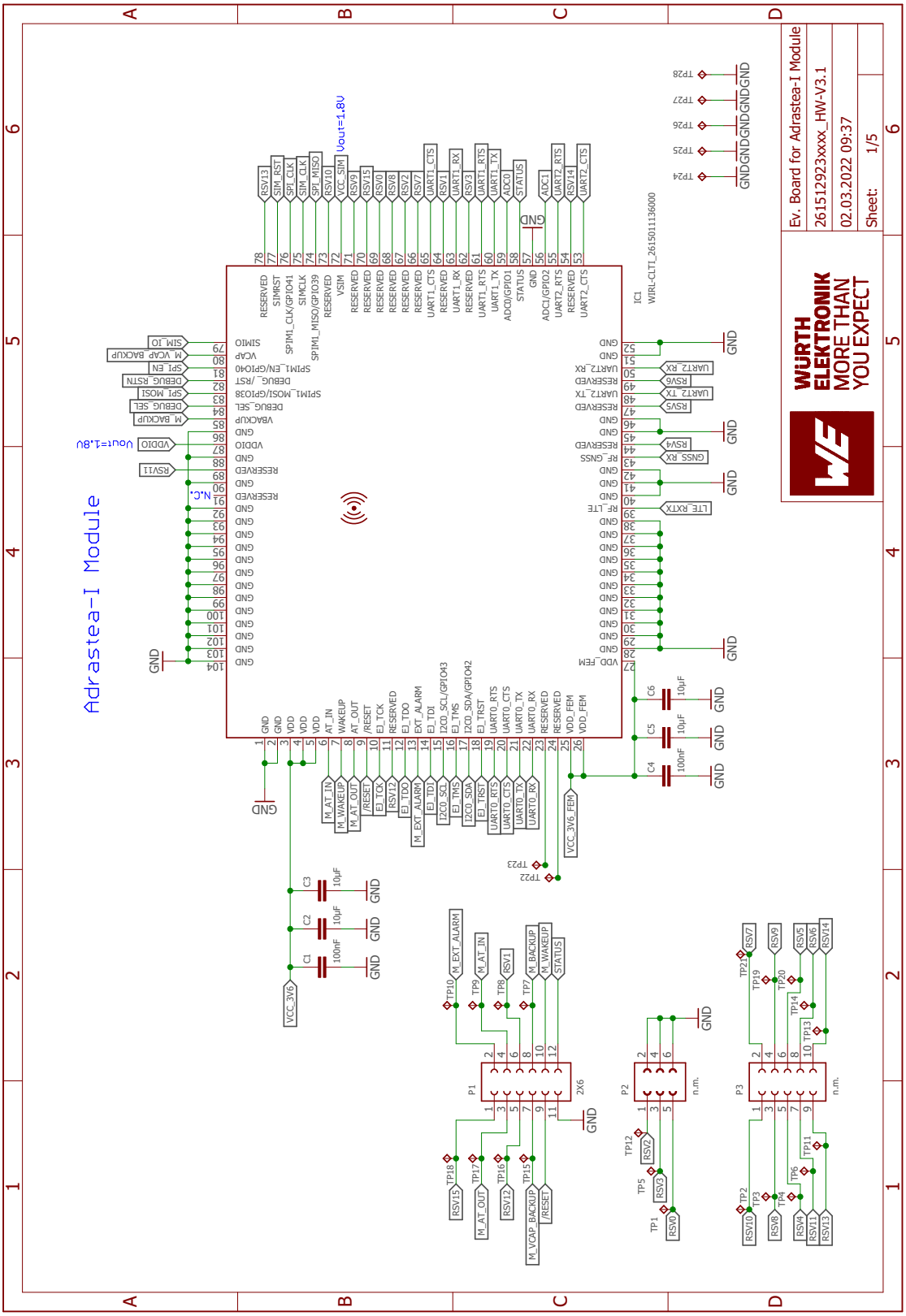


Figure 22: Circuit diagram 1

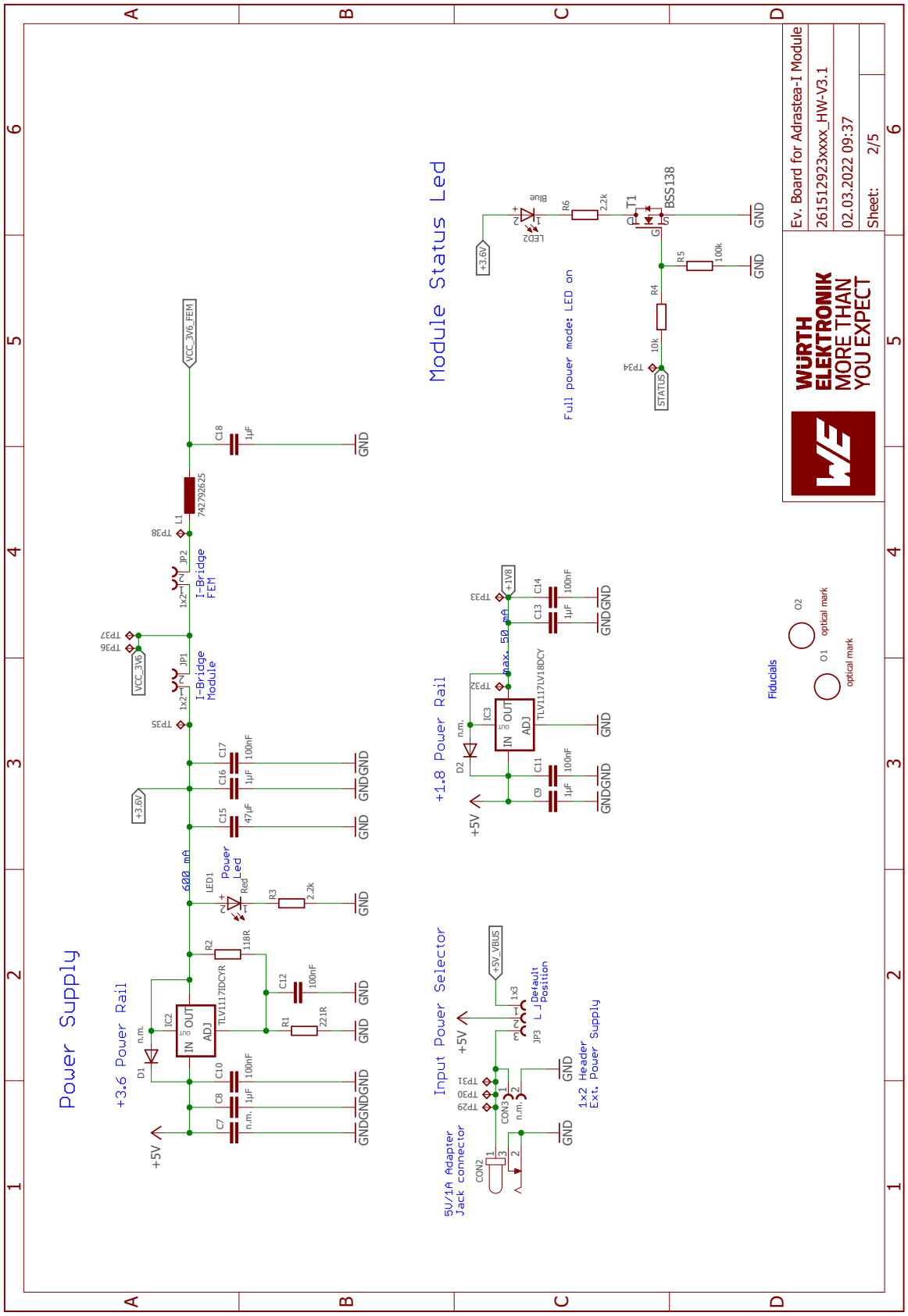


Figure 23: Circuit diagram 2

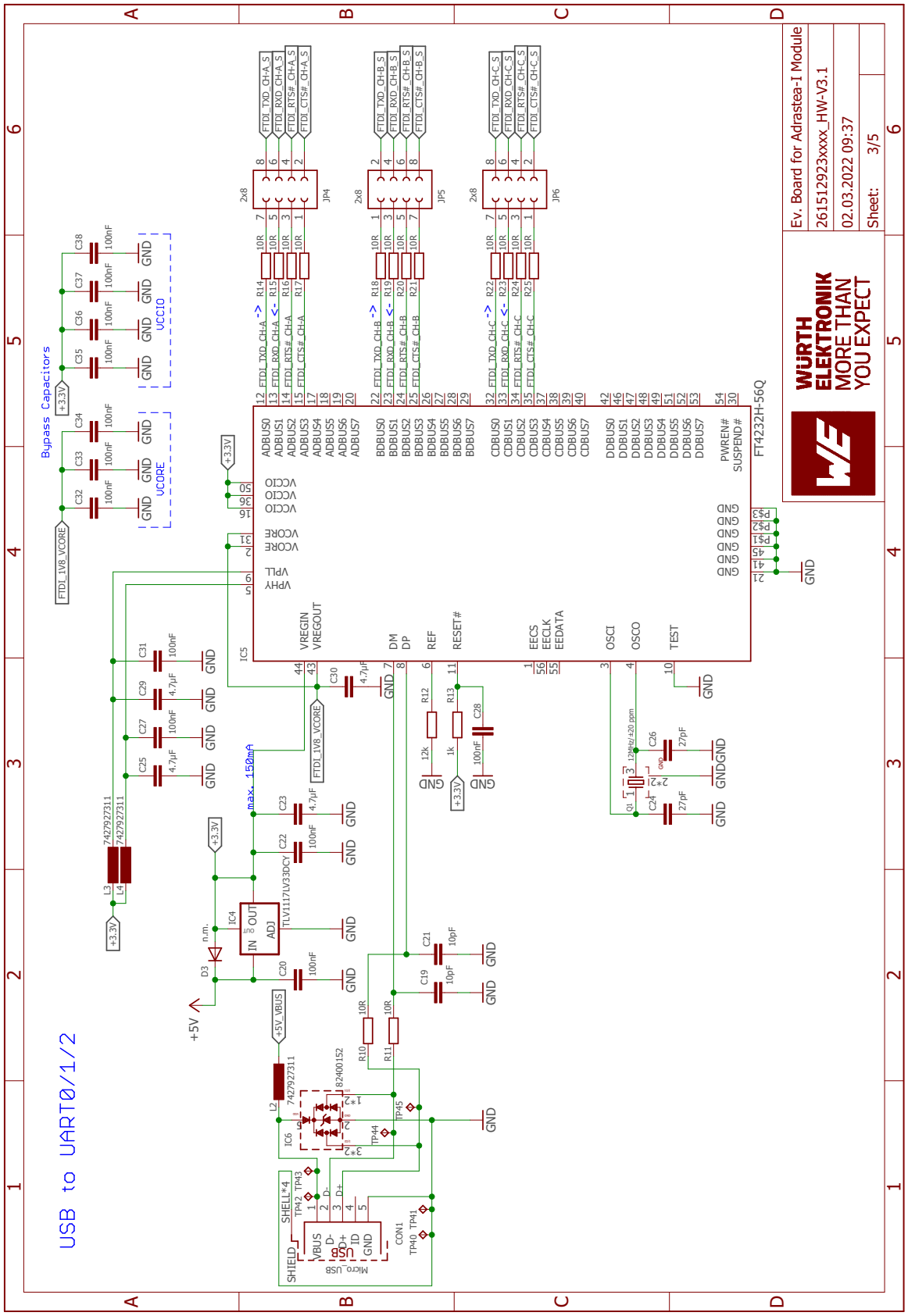


Figure 24: Circuit diagram 3

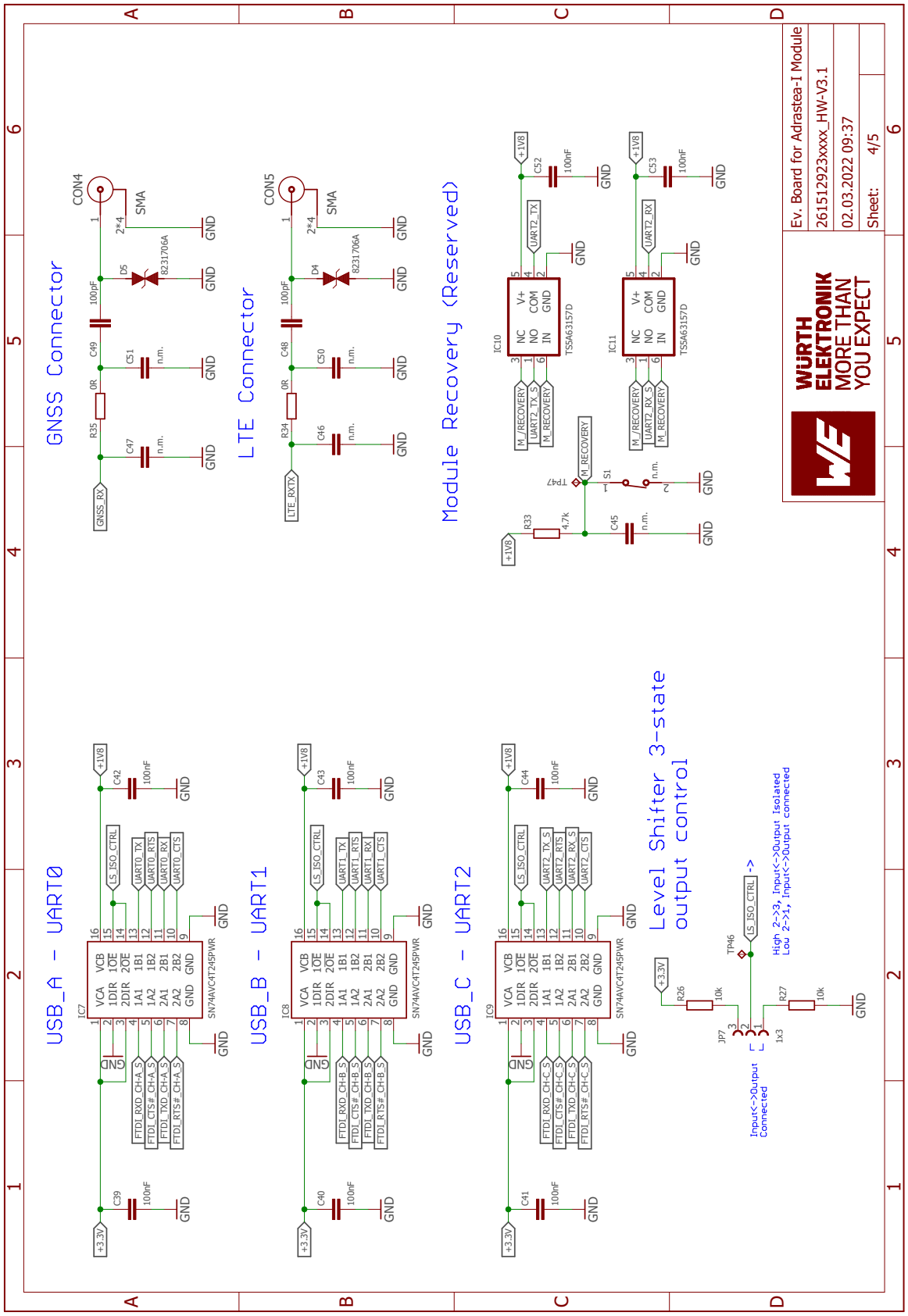


Figure 25: Circuit diagram 4

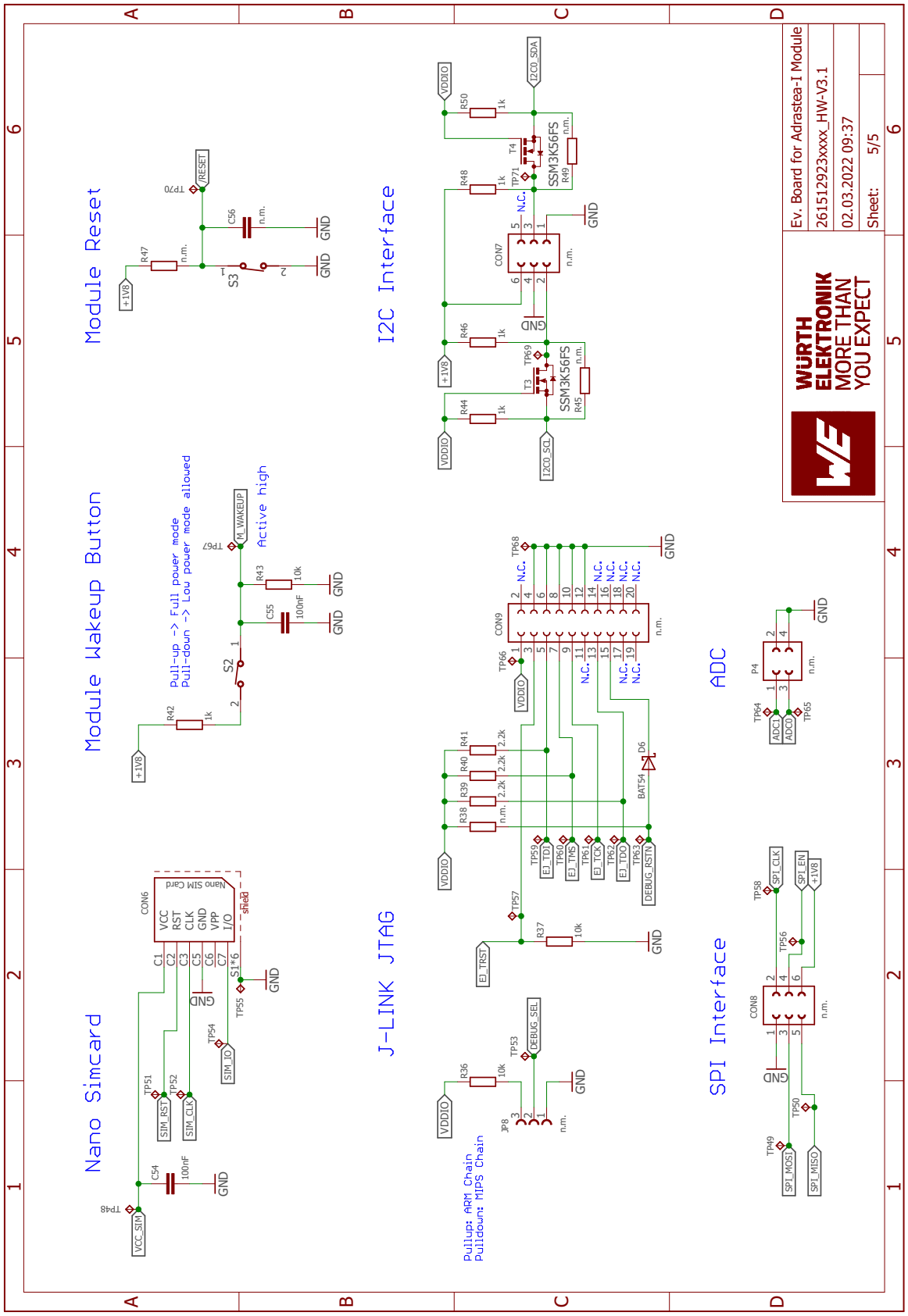


Figure 26: Circuit diagram 5

10.2 Layout

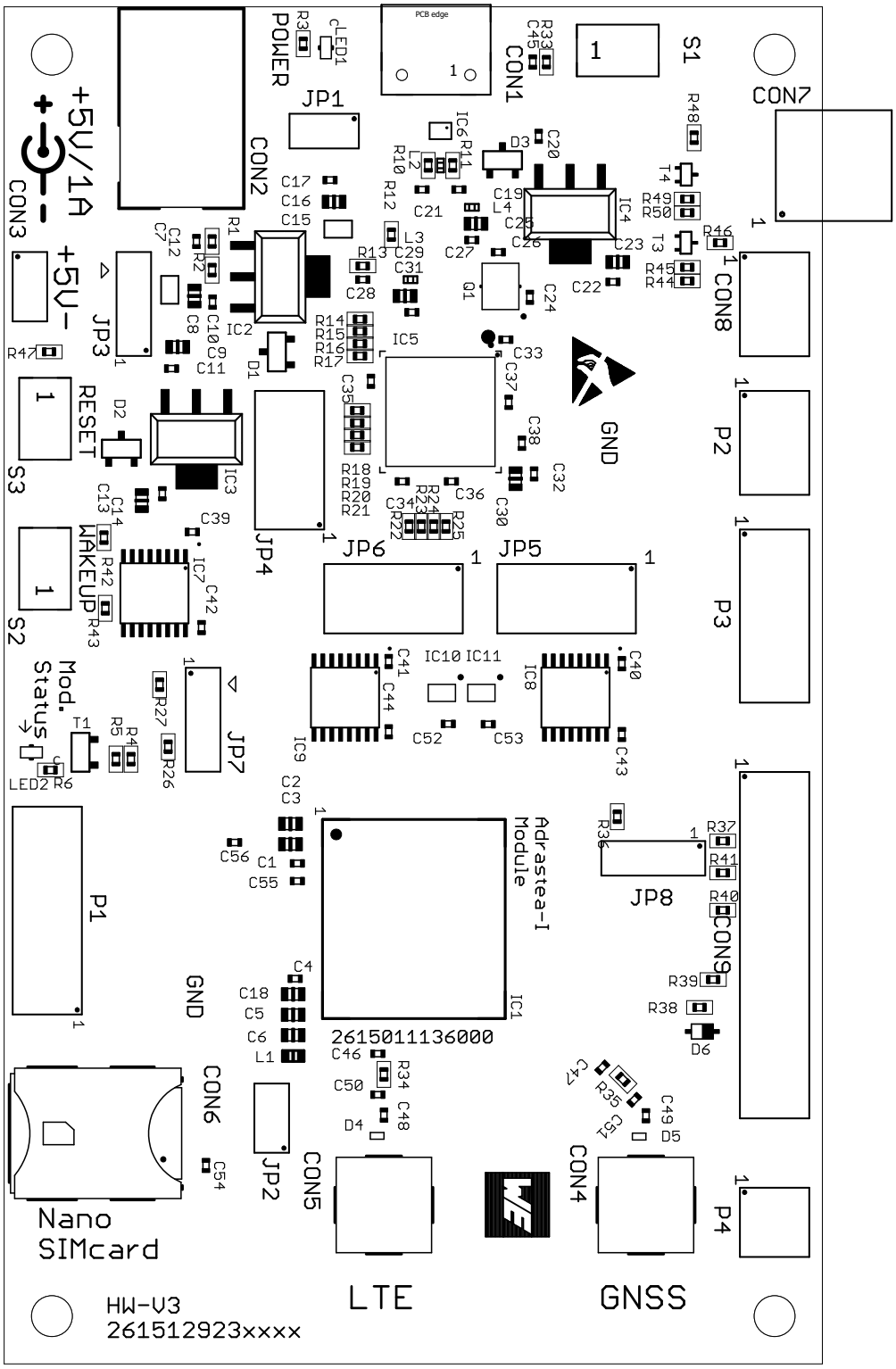


Figure 27: Assembly diagram

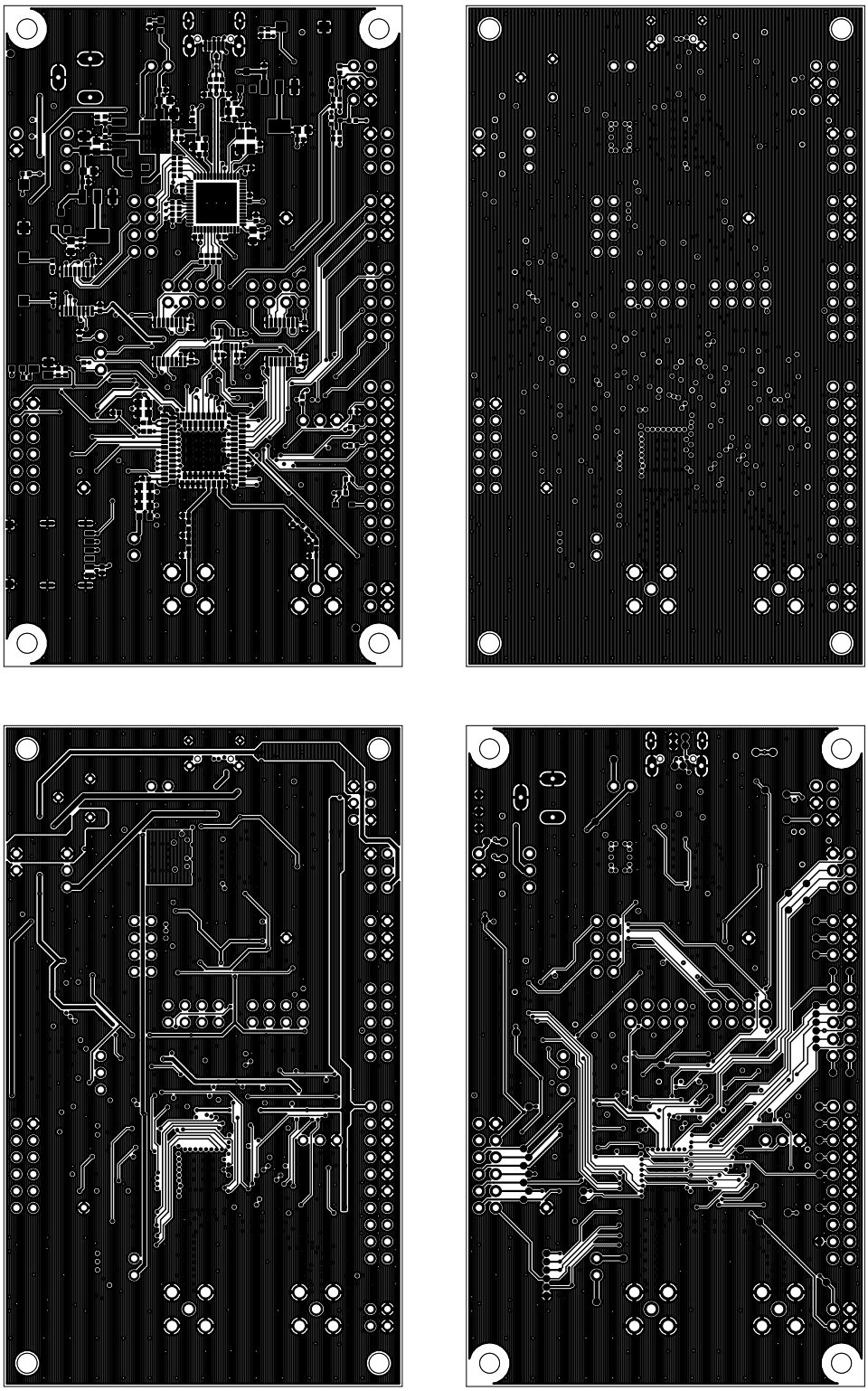


Figure 28: Top layer (upper left), second layer (upper right), third layer (bottom left), fourth layer (bottom right)

11 Manufacturing information

11.1 Moisture sensitivity level

This wireless connectivity product is categorized as JEDEC Moisture Sensitivity Level 3 (MSL3), which requires special handling.
More information regarding the MSL requirements can be found in the IPC/JEDEC J-STD-020 standard on *www.jedec.org*.
More information about the handling, picking, shipping and the usage of moisture/reflow and/or process sensitive products can be found in the IPC/JEDEC J-STD-033 standard on *www.jedec.org*.

11.2 Soldering

11.2.1 Reflow soldering

Attention must be paid on the thickness of the solder resist between the host PCB top side and the modules bottom side. Only lead-free assembly is recommended according to JEDEC J-STD020.

Profile feature		Value
Preheat temperature, min	$T_{S\ Min}$	150 °C
Preheat temperature, max	$T_{S\ Max}$	200 °C
Preheat time from $T_{S\ Min}$ to $T_{S\ Max}$	t_S	60 - 120 s
Ramp-up rate (T_L to T_P)		3 °C/s max.
Liquidous temperature	T_L	217 °C
Time t_L maintained above T_L	t_L	60 - 150 s
Peak package body temperature	T_P	245 °C
Time within 5 °C of actual peak temperature	t_P	20 - 30 s
Ramp-down rate (T_P to T_L)		6 °C/s max.
Time 20 °C to T_P		8 min max.

Table 37: Classification reflow soldering profile, Note: refer to IPC/JEDEC J-STD-020E

It is recommended to solder this module on the last reflow cycle of the PCB. For solder paste use a LFM-48W or Indium based SAC 305 alloy (Sn 96.5 / Ag 3.0 / Cu 0.5 / Indium 8.9HF / Type 3 / 89 %) type 3 or higher.

The reflow profile must be adjusted based on the thermal mass of the entire populated PCB, heat transfer efficiency of the reflow oven and the specific type of solder paste used. Based on the specific process and PCB layout the optimal soldering profile must be adjusted and verified. Other soldering methods (e.g. vapor phase) have not been verified and have to be validated by the customer at their own risk. Rework is not recommended.

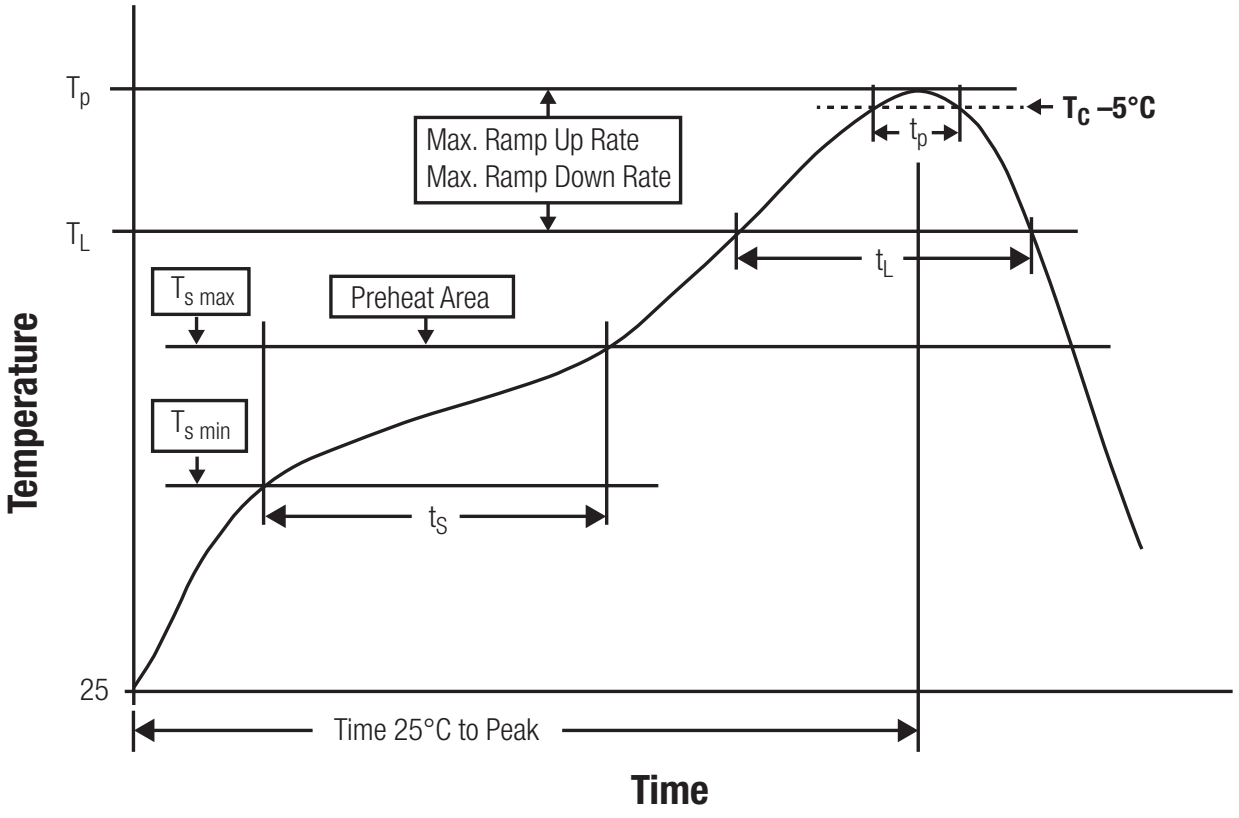


Figure 29: Reflow soldering profile

After reflow soldering, visually inspect the board to confirm proper alignment.

11.2.2 Cleaning

Do not clean the product. Any residue cannot be easily removed by washing. Use a "no clean" soldering paste and do not clean the board after soldering.

- Do not clean the product with water. Capillary effects can draw water into the gap between the host PCB and the module, absorbing water underneath it. If water is trapped inside, it may short-circuit adjoining pads. The water may also destroy the label and ink-jet printed text on it.
- Cleaning processes using alcohol or other organic solvents may draw solder flux residues into the housing, which won't be detected in a post-wash inspection. The solvent may also destroy the label and ink-jet printed text on it.
- Do not use ultrasonic cleaning as it will permanently damage the part, particularly the crystal oscillators.

11.2.3 Potting and coating

- If the product is potted in the customer application, the potting material might shrink or expand during and after hardening. Shrinking could lead to an incomplete seal, allowing contaminants into the component. Expansion could damage components. We recommend a manual inspection after potting to avoid these effects.
- Conformal coating or potting results in loss of warranty.
- The RF shield will not protect the part from low-viscosity coatings and potting. An undefined amount of coating and potting will enter inside the shielding.
- Conformal coating and potting will influence the parts of the radio front end and consequently influence the radio performance.
- Potting will influence the temperature behavior of the device. This might be critical for components with high power.

11.2.4 Other notations

- Do not attempt to improve the grounding by forming metal strips directly to the EMI covers or soldering on ground cables, as it may damage the part and will void the warranty.
- Always solder every pad to the host PCB even if some are unused, to improve the mechanical strength of the module.
- The part is sensitive to ultrasonic waves, as such do not use ultrasonic cleaning, welding or other processing. Any ultrasonic processing will void the warranty.

11.3 ESD handling

This product is highly sensitive to electrostatic discharge (ESD). As such, always use proper ESD precautions when handling. Make sure to handle the part properly throughout all stages of production, including on the host PCB where the module is installed. For ESD ratings, refer to the module series' maximum ESD section. For more information, refer to the relevant chapter 4. Failing to follow the aforementioned recommendations can result in severe damage to the part.

- The first contact point when handling the PCB is always between the local GND and the host PCB GND, unless there is a galvanic coupling between the local GND (for example work table) and the host PCB GND.
- Before assembling an antenna patch, connect the grounds.
- While handling the RF pin, avoid contact with any charged capacitors and be careful when contacting any materials that can develop charges (for example coaxial cable with around 50-80 pF/m, patch antenna with around 10 pF, soldering iron etc.)
- Do not touch any exposed area of the antenna to avoid electrostatic discharge. Do not let the antenna area be touched in a non ESD-safe manner.
- When soldering, use an ESD-safe soldering iron.

11.4 Safety recommendations

It is your duty to ensure that the product is allowed to be used in the destination country and within the required environment. Usage of the product can be dangerous and must be tested and verified by the end user. Be especially careful of:

- Use in areas with risk of explosion (for example oil refineries, gas stations).
- Use in areas such as airports, aircraft, hospitals, etc., where the product may interfere with other electronic components.

It is the customer's responsibility to ensure compliance with all applicable legal, regulatory and safety-related requirements as well as applicable environmental regulations. Disassembling the product is not allowed. Evidence of tampering will void the warranty.

- Compliance with the instructions in the product manual is recommended for correct product set-up.
- The product must be provided with a consolidated voltage source. The wiring must meet all applicable fire and security prevention standards.
- Handle with care. Avoid touching the pins as there could be ESD damage.

Be careful when working with any external components. When in doubt consult the technical documentation and relevant standards. Always use an antenna with the proper characteristics.

Würth Elektronik eiSos radio modules with high output power of up to 500 mW generate a large amount of heat while transmitting. The manufacturer of the end device must take care of potentially necessary actions for his application.

12 Product testing

12.1 Würth Elektronik eiSos in-house production tests

To achieve a high quality standard, Würth Elektronik eiSos follows a philosophy of supplying fully tested radio modules. At the end of the production process, every unit undergoes an optical inspection. Here the quality of soldering, edge castellation and edge milling is monitored.

If this has been passed, the radio modules are handed over to the automatic test equipment for the electrical characterization. This includes:

- Voltage and current tests to ensure proper electrical performance
- RF characteristics (frequency, spectrum, TX power) measurement and calibration
- Radio communication tests
- Firmware and serial number programming
- Host interface communication tests

The automated testing process is logged for internal quality control. The gained measurement data of each unit is analysed to detect defective parts and investigate the corresponding root cause. Defective radio modules are discarded, in order to guarantee a 100% failure-free delivery to customers.

12.2 EMS production tests

The rigorous in-series production testing ensures that EMS don't need to duplicate firmware tests or measurements. This streamlines the process and eliminates the need for additional testing over analogue and digital interfaces during device production. When it comes to device testing, the ideal focus should be on module assembly quality:

- All module pins are soldered properly on the base PCB
- There are no short circuits
- The mounting process did not damage the module
- The communication between host and radio module is working
- The antenna is connected properly

Simple "Go/No go" tests, like checking the RSSI value, give already a hint if the power supply and antenna have been connected properly.

In addition to such standard testing procedures, radio module integrators have the flexibility to perform additional dedicated tests to thoroughly evaluate the device. Specific tests they can consider are:

- Measure module current consumption in a specified operating state. Deviations from expected results (compared to a "Golden Device") can signal potential issues.

- Perform functional tests, including communication checks with the host controller and verification of interfaces.
- Assess fundamental RF characteristics (modulation accuracy, power levels, spectrum). Verify that the device meets expected performance standards.

13 Physical specifications

13.1 Dimensions

Dimensions
13.4 * 14.6 * 1.85 mm

Table 38: Dimensions

Tolerances: see chapter 13.3

13.2 Weight

Weight
0.80 g

Table 39: Weight

Tolerance: ± 0.15 g

13.3 Module drawing

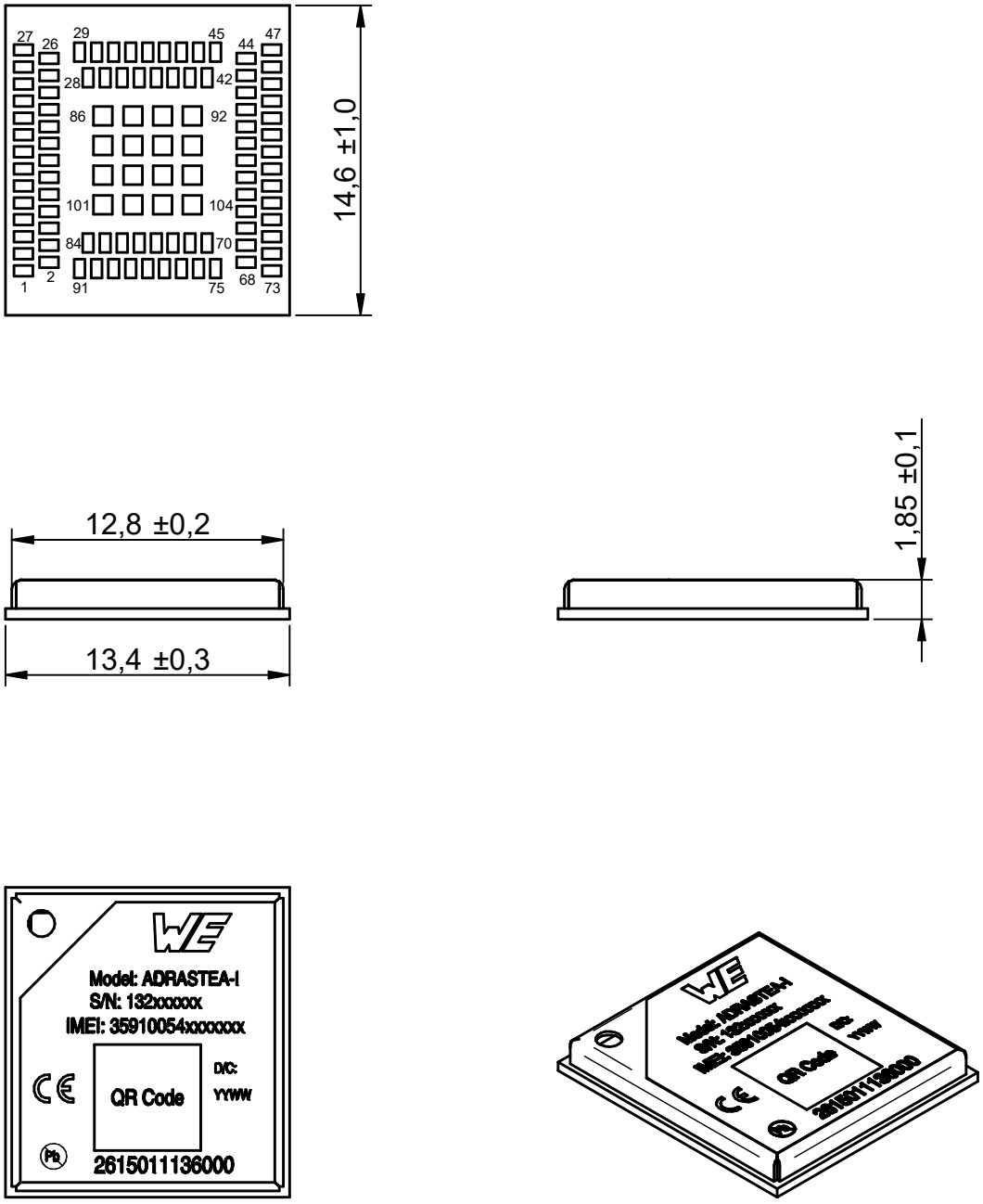


Figure 30: Module dimensions [mm]

13.4 Footprint

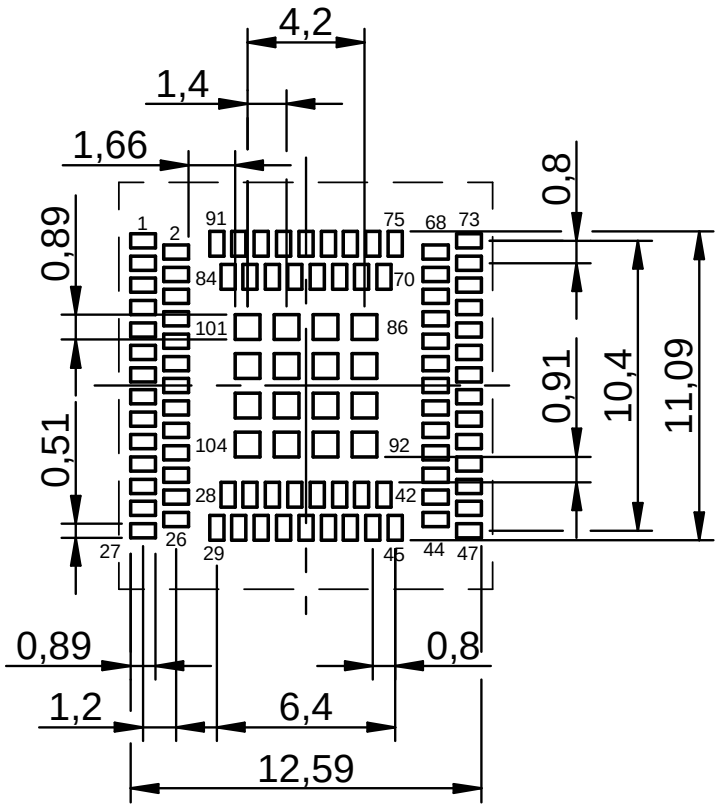


Figure 31: Footprint and dimensions [mm]

14 Marking

14.1 Lot number

The lot number is printed in numerical digits as well as in form of a machine readable bar code. It is divided into blocks as shown in the following picture and can be translated according to the following table.

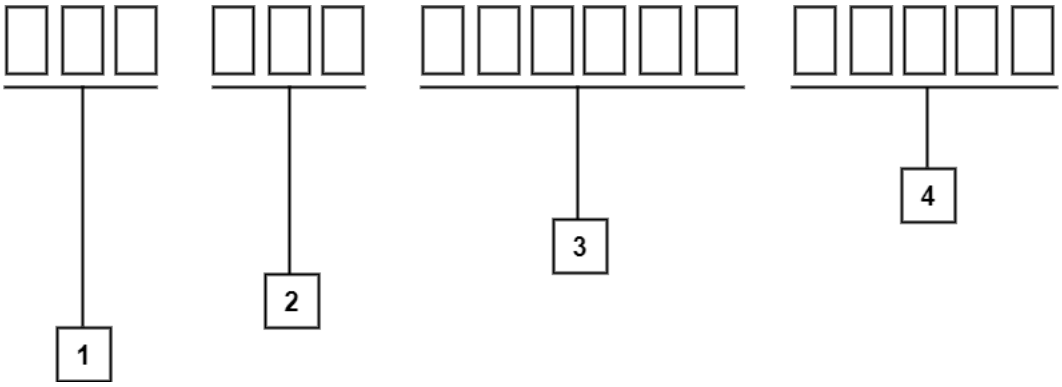


Figure 32: Lot number structure

Block	Information	Example(s)
1	eiSos internal, 3 digits	627
2	eiSos internal, 3 digits	DGW
3	Date code in YYMMDD, 6 digits	211222 where YY:21, MM:12, DD:22
4	eiSos internal (Optional), 5 digits	-

Table 40: Lot number details

Adrastea-I has different firmware versions for the MCU FW and the Modem FW. To obtain the complete firmware version, use the AT%VER AT command.

14.2 General labeling information

Labels of Würth Elektronik eiSos radio modules include several fields. Besides the manufacturer identification, the product's *WE* order code, serial number and certification information are placed on the label. In case of small labels, additional certification marks are placed on the label of the reel.
The information on the label are fixed. Only the serial number changes with each entity of the radio module. For Adrastea-I the label is as follows:

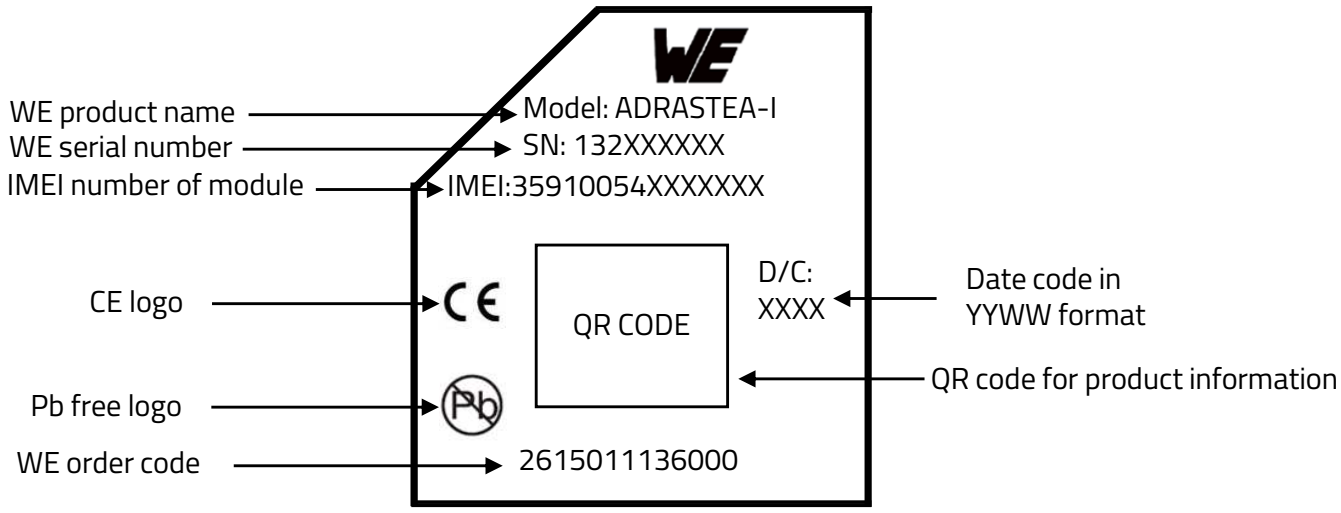


Figure 33: Label of the Adrastea-I

15 Information for explosion protection

In case the end product should be used in explosion protection areas the following information can be used:

- The module itself has no internal fuse.
- The maximum output power of the module is 25.7 dBm.
- The total amount of capacitance of all capacitors is 49.23 µF.
- The total amount of inductance of all inductors is 2.22 µH.

16 Regulatory compliance information

16.1 Important notice EU

The use of RF frequencies is limited by national regulations. The Adrastea-I has been designed to comply with the RED directive 2014/53/EU of the European Union (EU).
The Adrastea-I can be operated without notification and free of charge in the area of the European Union. However, according to the RED directive, restrictions (e.g. in terms of duty cycle or maximum allowed RF power) may apply.

Modifications (2014/53/EU article 3 (i))
Caution: Changes or modifications for this equipment not expressly approved by Würth Elektronik eiSos may void the CE conformity to operate this equipment.

Since the module is a built-in equipment its power class according to EN 62368-1 must be specified in the end product.

16.2 Important notice UKCA

The UK's government has laid legislation to continue recognition of current EU requirements for a range of product regulations, including the CE marking. The Radio Equipment Regulation 2017/1206 is within the scope of this announcement, among others.
Consequently, the Adrastea-I can be sold and utilized in the UK with the CE marking, without the need of UKCA declaration of conformity or UKCA marking.

Source: *https://www.gov.uk/guidance/ce-marking*

16.3 Conformity assessment of the final product

The Adrastea-I is a subassembly. It is designed to be embedded into other products (products incorporating the Adrastea-I are henceforward referred to as "final products").
It is the responsibility of the manufacturer of the final product to ensure that the final product is in compliance with the essential requirements of the underlying national radio regulations.
The conformity assessment of the subassembly Adrastea-I carried out by Würth Elektronik eiSos does not replace the required conformity assessment of the final product.

16.4 Exemption clause

Relevant regulation requirements are subject to change. Würth Elektronik eiSos does not guarantee the accuracy of the before mentioned information. Directives, technical standards, procedural descriptions and the like may be interpreted differently by the national authorities. Equally, the national laws and restrictions may vary with the country. In case of doubt or uncertainty, we recommend that you consult with the authorities or official certification organizations

of the relevant countries. Würth Elektronik eiSos is exempt from any responsibilities or liabilities related to regulatory compliance.

Notwithstanding the above, Würth Elektronik eiSos makes no representations and warranties of any kind related to their accuracy, correctness, completeness and/or usability for customer applications. No responsibility is assumed for inaccuracies or incompleteness.

16.5 EU Declaration of conformity

EU DECLARATION OF CONFORMITY

Radio equipment: **Adrastea-I**

The manufacturer: Würth Elektronik eiSos GmbH & Co. KG
Max-Eyth-Straße 1
74638 Waldenburg

This declaration of conformity is issued under the sole responsibility of the manufacturer.

Object of the declaration: Adrastea-I

The object of the declaration described above is in conformity with the relevant Union harmonisation legislation Directive 2014/53/EU. Following harmonised norms or technical specifications have been applied:

EN 301 908-1 V15.2.1 (2023-01)
EN 301 908-13 V13.2.1 (2022-02)
EN 303 413 V1.2.1 (2021-04)
EN 301 489-1 V2.2.3 (2019-11)
EN 301 489-19 V2.1.1 (2019-04)
EN 301 489-52 V1.2.1 (2021-11)
EN 62311: 2008
EN 62368-1: 2014/AC: 2015/A11: 2017
2011/65/EU with its amending Annex II EU 2015/863

i.A. G. Eßlandt

Trier, 2nd of February 2025
Place and date of issue

16.6 RED-DA Cybersecurity statement

This chapter addresses cybersecurity requirements as per Articles 3.3d, 3.3e, and 3.3f of the Radio Equipment Directive Delegated Act (RED-DA). Compliance with RED-DA can be achieved by adhering to the following standards, if applicable:

- EN 18031-1: Common security requirements for radio equipment - Part 1: Internet connected radio equipment
- EN 18031-2: Common security requirements for radio equipment - Part 2: Radio equipment processing data, namely internet connected radio equipment, childcare radio equipment, toys radio equipment and wearable radio equipment
- EN 18031-3: Common security requirements for radio equipment - Part 3: Internet connected radio equipment processing virtual money or monetary value

The Adrastea-I module, in its delivered form, is a sub-component that cannot connect to or interact with the internet independently. It lacks a SIM card and a host microcontroller or application firmware, both of which are required to initiate a cellular connection which in turn provides the option to trigger a connection with the cellular network and with the internet.

This leads to the following RED-DA statement for the component Adrastea-I:

Requirements of RED-DA 3.3	Statement and conditions
(d) Radio equipment does not harm the network or its functioning nor misuses network resources, thereby causing an unacceptable degradation of service	"Not applicable": The Adrastea-I does not pose a risk towards the requirement of RED-DA 3.3d, since it cannot connect or interact with the internet in the extent of delivery.
(e) Radio equipment incorporates safeguards to ensure that the personal data and privacy of the user and of the subscriber are protected	"Not applicable": The product does not pose a risk to the user's or subscriber's privacy, as it does not store or process any personal data. It also cannot connect or interact with the internet in the extent of delivery.
(f) Radio equipment supports certain features ensuring protection from fraud	"Not applicable": The product does not pose a risk of fraud because it does not store or process financial data or enables financial transactions. It also cannot connect or interact with the internet in the extent of delivery.

16.7 RED-DA Cybersecurity first actions

Designers and manufacturers of products using radio communication may consider the following decision graphs to assess whether RED-DA applies to their product or not. The RED-DA, if applicable, requires specific conditions to be fulfilled to allow a Self-Assessment.

The RED-DA harmonized norm series (EN 18031) are not free of charge and need to be purchased.

These decision graphs are not a substitute for buying, reading, understanding and applying the norms and the RED-DA requirements and conditions.

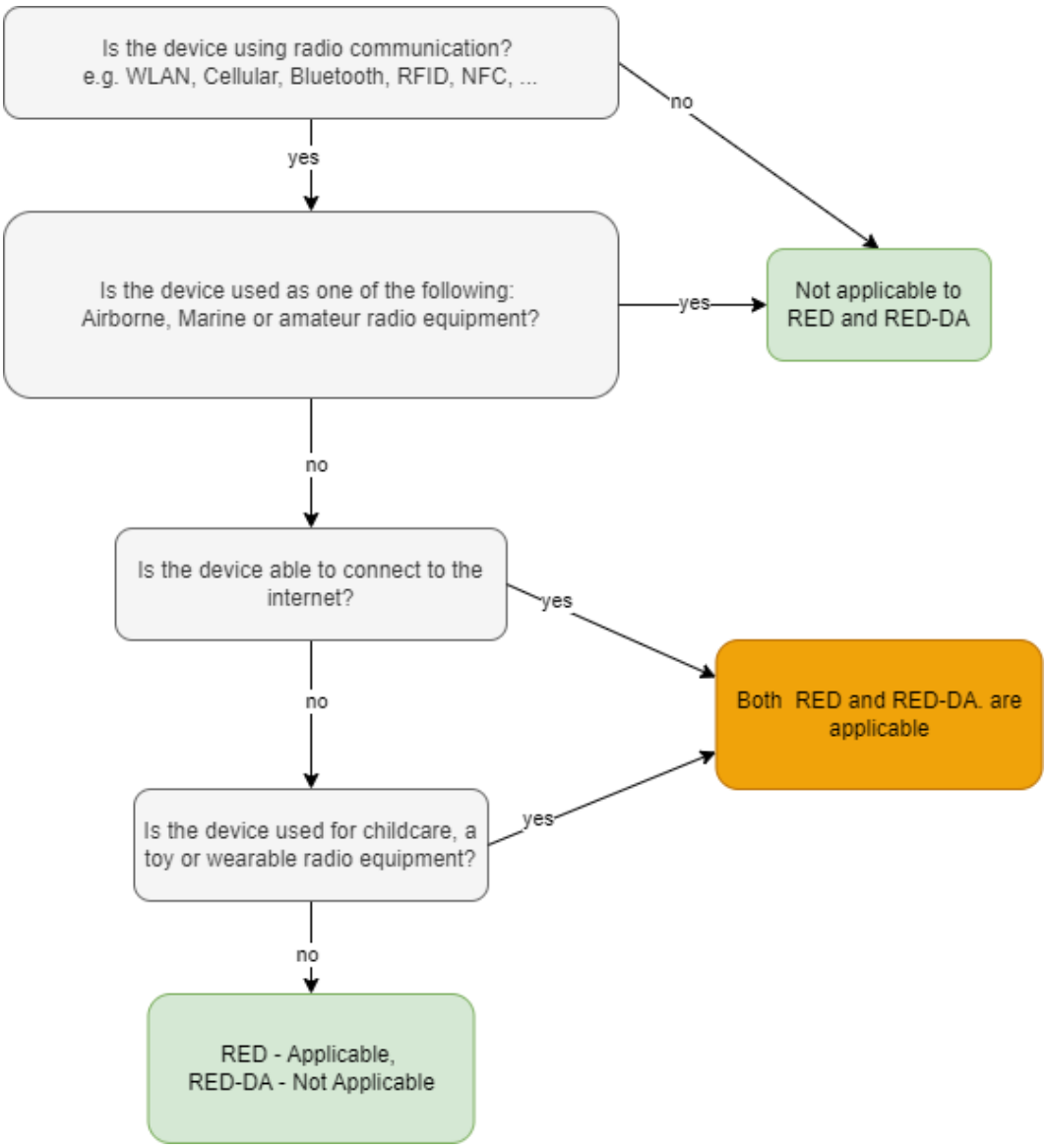


Figure 34: RED and/or RED-DA?

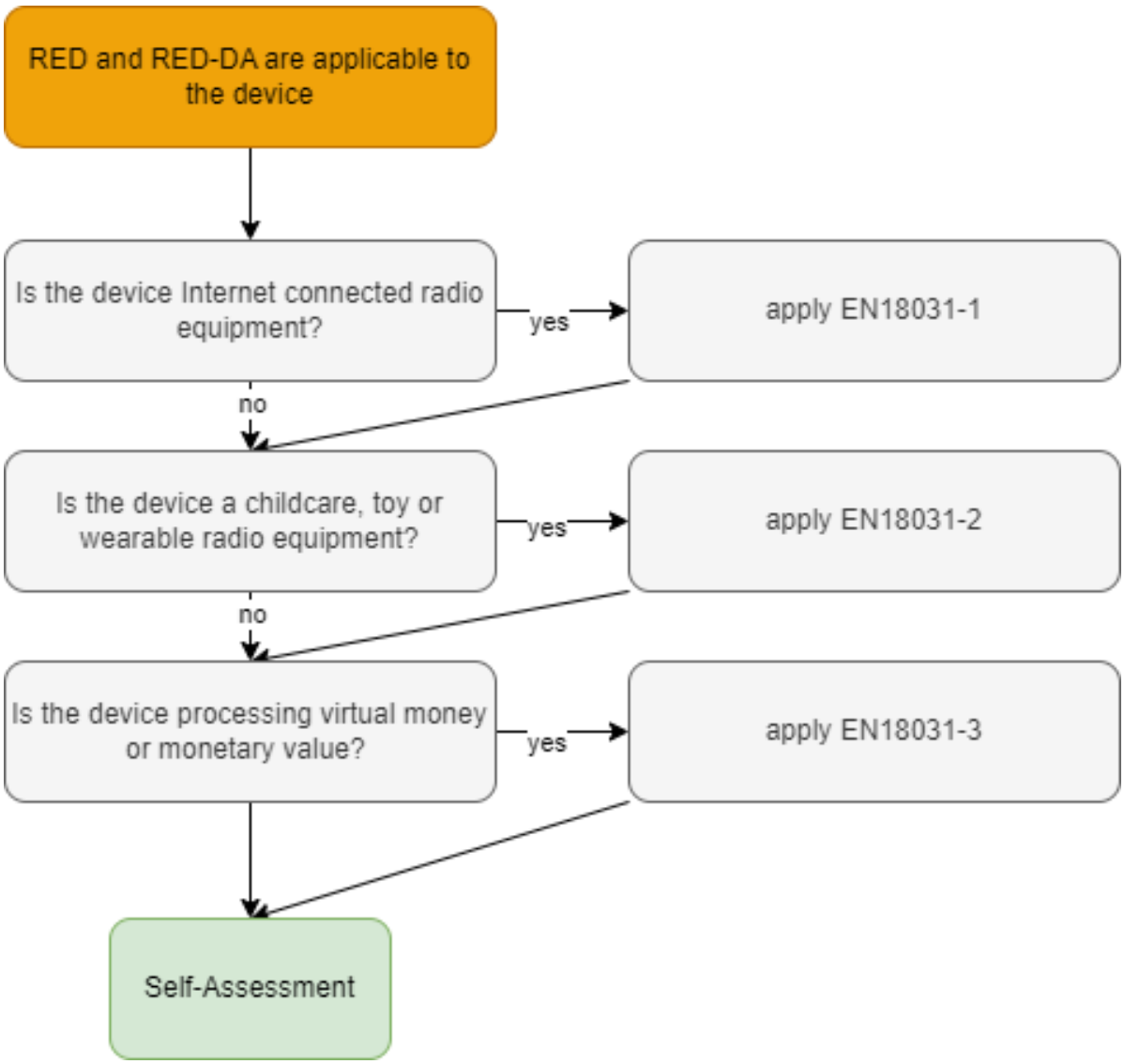


Figure 35: Which parts of RED-DA?

16.8 RED-DA Cybersecurity guideline for end devices using Adrastea-I

If the Adrastea-I is integrated into an end device, the application may include the necessary components to connect to a cellular network and the internet. This may make the RED-DA 3.3d, e, f and EN 18031-1, -2, -3 "applicable".

It is essential to go through the following steps to ensure conformity to the RED-DA

1. Risk assessment
2. Testing
3. Declaration of Conformity (DoC)

The first step in the process of risk assessment is the identification of the assets present in the end device. The table below summarizes the type of assets and their applicability to the corresponding standards.

Requirement	3.3d	3.3e	3.3f
Security asset	X	X	X
Network asset	X		
Privacy asset		X	
Financial asset			X

Table 42: Cybersecurity Assets

Once the assets are listed, a risk assessment needs to be performed by going through the decision trees specified in the corresponding EN 18031 standard for every asset in the list and documenting the justifications for each decision made. This is the technical documentation based on which conceptual as well as functional assessment needs to be performed before declaring conformity.
Based on the configuration, the Adrastea-I module adds the following assets to the list of the end product.

Network assets

- Cellular interface (APN)
- TCP Client
- UDP Client
- TLS Client
- dTLS Client
- MQTT over TLS Client
- HTTPS Client for FOTA (firmware update)
- HTTPS Client for user application
- CoAP Client
- DNS Client
- DHCP Client
- ARP
- ICMP (Ping)

Security assets

- IMEI
- Credentials to use the SIM card
- Credentials for TLS (Certificate, private key)
- Credentials for HTTP (User name, password, certificate, private key)
- Credentials for MQTT (User name, password, certificate, private key)
- Credentials for CoAP (User name, password, certificate, private key)

For applicable radio modules Würth Elektronik eiSos provides pre-filled risk assessment templates that can be extended to create technical documentation for the end application. Contact *wcs@we-online.com* or your local sales representative for more information on how to get access to this documentation.

17 References

[1] Würth Elektronik. Adrastea Commander. http://www.we-online.com/Adrastea-Commander.

[2] Würth Elektronik. ADRASTEA-I EVALUATION BOARD MANUAL. https://we-online.com/katalog/en/manual/2615029236001.

18 Important notes

The following conditions apply to all goods within the wireless connectivity and sensors product range of Würth Elektronik eiSos GmbH & Co. KG:

General customer responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact, it is up to the customer to evaluate, where appropriate to investigate and to decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the documentation is current before placing orders.

Customer responsibility related to specific, in particular safety-relevant applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. The same statement is valid for all software source code and firmware parts contained in or used with or for products in the wireless connectivity and sensor product range of Würth Elektronik eiSos GmbH & Co. KG. In certain customer applications requiring a high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health, it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

Best care and attention
Any product-specific data sheets, manuals, application notes, PCNs, warnings and cautions must be strictly observed in the most recent versions and matching to the products revisions. These documents can be downloaded from the product specific sections on the wireless connectivity and sensors homepage.

Customer support for product specifications
Some products within the product range may contain substances, which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case, the Business Development Engineer (BDM) or the internal sales person in charge should be contacted who will be happy to support in this matter.

Product improvements
Due to constant product improvement, product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard, we inform about major changes. In case of further queries regarding the PCN, the Business Development Engineer (BDM), the internal sales person or the technical support team in charge should be contacted. The basic responsibility of the customer as per section 18 and 18 remains unaffected.
All software like ¨wireless connectivity SDK¨, ¨Sensor SDK¨ or other source codes as well as all PC software tools are not subject to the Product Change Notification information process.

Product life cycle
Due to technical progress and economical evaluation, we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this, we cannot ensure that all products within our product range will always be available. Therefore, it needs to be verified with the Business Development Engineer (BDM) or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

Property rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

General terms and conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the "General Terms and Conditions of Würth Elektronik eiSos Group", last version available at *www.we-online.com*.

19 Legal notice

Exclusion of liability
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List of Figures

List of Tables

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